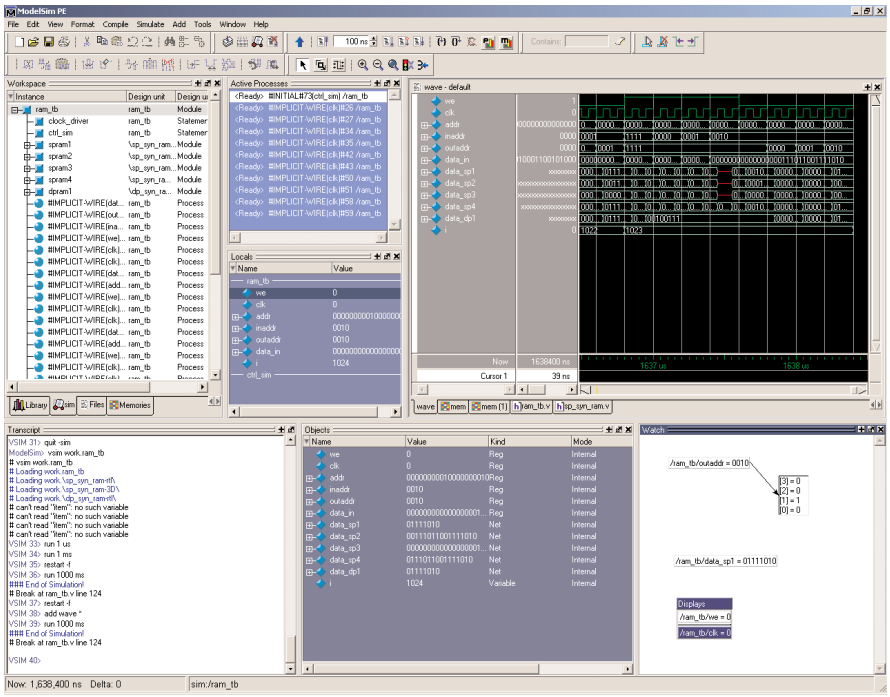
ModelSim PE

D A T A S H E E T



ModelSim PE is the industry-leading, Windows-based simulator for VHDL, Verilog, or mixed-language simulation environments.

Major product features:

- Optimized Native Compiled architecture
- Single Kernel Simulator technology
- VHDL, Verilog, and mixed-language simulation
- Intelligent, easy-to-use GUI with Tcl interface
- Full support for Verilog 2001
- SystemVerilog design
- Waveform File Manager (wlfman)
- Project manager and source code templates and wizards
- Memory window, Signal Spy™
- Windows® platform support
- Options: SystemC, SWIFT Interface support, graphics-based Dataflow window, Waveform Compare, integrated code coverage, Profiler (for more details on options, please see the ModelSim SE datasheet)

ModelSim® PE, our entry-level simulator, offers VHDL, Verilog, or mixed-language simulation. Coupled with the most popular HDL debugging capabilities in the industry, ModelSim PE is known for delivering high performance, ease of use, and outstanding product support.

Model Technology's award-winning Single Kernel Simulation (SKS) technology enables transparent mixing of VHDL and Verilog in one design. ModelSim's architecture allows platform independent compile with the outstanding performance of native compiled code.

An easy-to-use graphical user interface enables you to quickly identify and debug problems, aided by dynamically updated windows. For example, selecting a design region in the Structure window automatically updates the Source, Signals, Process, and Variables windows. These cross linked ModelSim windows create a powerful easy-to-use debug environment. Once a problem is found, you can edit, recompile, and re-simulate without leaving the simulator.

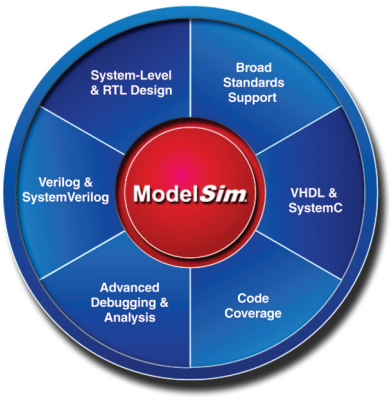
ModelSim PE fully supports the VHDL and Verilog language standards. You can simulate behavioral, RTL, and gate-level code separately or simultaneously. ModelSim PE also supports all ASIC and FPGA libraries, ensuring accurate timing simulations. ModelSim PE provides initial support for VHDL 2002.

A More Intelligent GUI

An intelligently engineered GUI makes efficient use of desktop real estate. The intuitive arrangement of interactive graphical elements (windows, toolbars, menus, etc.) makes it easy to view and access the many powerful capabilities of ModelSim. The result is a feature-rich GUI that is easy to use and quickly mastered. ModelSim redefined openness in simulation by incorporating the Tcl user interface into its HDL simulator. Tcl is a simple but powerful scripting language for controlling and extending applications.

ModelSim®

Mentor Graphics®



Verilog 2001/SystemVerilog

ModelSim PE now fully supports IEEE 1364-2001, including SystemVerilog design language features. SystemVerilog is an Accellera standard that provides new constructs for modeling at higher levels of abstraction.

Memory Window

Allows flexible viewing and changing of memory locations. VHDL and Verilog memories are auto extracted in the GUI allowing powerful search, fill, load and save functionality. Memory Window allows pre-loading of memories thus saving the time consuming step of initializing sections of your simulations just to load memories. All functions are available via the command line allowing their use in scripting.

Waveform File Manager (wlfman)

This utility allows the manipulation of existing *wlf* files so you can reduce the amount of information to display. You can view a portion of the original waveform file and modify time scales to compare RTL versus gates.

Source Window Templates and Wizards

VHDL and Verilog templates and wizards allow you to quickly develop HDL code without having to remember the exact language syntax. All the language constructs are available with a click of a mouse. Easy-to-use wizards step you through creation of more complex HDL blocks. The wizards show you how to create parameterizable logic blocks, testbench stimuli, and design objects. The source window templates and wizards benefit both novice and advanced HDL developers with time-saving shortcuts.

Project Manager

The Project Manager greatly reduces the time it takes to organize files and libraries. As you compile and simulate, the Project Manager stores the unique settings of each individual project, allowing you to restart the simulator right where you left off. Simulation properties allow you to easily re-simulate with pre-configured parameters.

Signal Spy

From any point in the design, the Signal Spy feature allows you to monitor, drive, force, and release signals and signal nets buried deep in a VHDL or mixed-language design hierarchy. This can be done without having to modify any of your design's existing code. This feature is very useful in testbench design.

Complete Product Support and Maintenance

Model Technology provides the highest levels of support in the industry with our unique *Engineer of the Week* approach. You receive support from the engineers who design the ModelSim products. A standard annual maintenance contract provides technical support, maintenance releases, the *Informant* email newsletter, and access to on-line support and technical services.

Platform and Standards Support

ModelSim PE supports both VHDL and Verilog and accelerates VITAL functions, procedures and timing checks. ModelSim PE runs on the Windows 98, 2000, NT, XP, and ME platforms.

ModelSim LE Upgrade

For applications requiring the Linux platform, ModelSim PE users can upgrade to ModelSim LE. ModelSim LE is Verilog only.

ModelSim SE Upgrade

For applications requiring the highest simulation performance and advanced verification capabilities, ModelSim PE users can upgrade to ModelSim SE. ModelSim SE includes the same user interface as ModelSim PE, which eliminates any learning curve and ensures instant productivity. For more information, see the ModelSim SE datasheet.

Visit our web site at www.model.com for the latest product news.

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