

Vista IDE and debugging toolset for creating new SystemC designs or linking with existing SystemC and mixed language flows and kernels.

SystemC Design and Debug

SystemC is today's language of choice for system-level design and verification. Traditionally designers have used C++ software Integrated Development Environments (IDEs) to develop and debug their SystemC models, however these do not support hardware design concepts.

Vista™ is a state-of-the-art source-based SystemC debug toolset, providing powerful hardware and C/C++ oriented views and debugging mechanisms. The unique introspection browsers allow designers to efficiently trace C/C++ code structures and execution within a familiar hardware debugging platform. Vista naturally links into any existing SystemC design or testbench environments, plugs with most mixed-language kernels, and substantially improves design and verification productivity.

Unique HW and C/C++ Views on the Same Code

Vista Data Introspection browsers provide both hardware module hierarchy and C/C++ class hierarchy views of the design, enabling designers to better understand and debug their SystemC designs. Vista provides advanced coding facilities, browsers, and debug capabilities which can be applied to both the hardware and C/C++ views and allow intuitive insight into the model behavior throughout its hierarchy and execution flow.

Transaction Viewer for Transaction-Level Modeling

Vista provides a TLM viewer which captures the interface method calling sequence and presents the communication protocol transactions in an intuitive tabular format.

Features

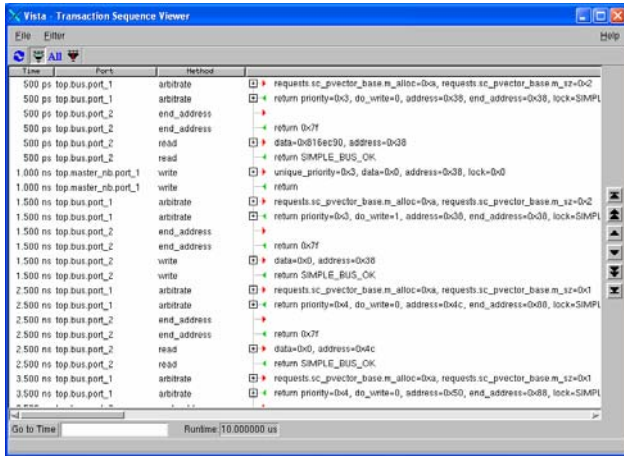
- Advanced SystemC debug platform
- Enables switching HW (hierarchy) and C++ (class inheritance) views, tightly linked with the source code
- Unique TLM transaction viewer
- Process runtime status (9 statuses)
- Instantly displays stack and local variables value for every process
- Variables and C/C++ objects tracing in waveform
- Waveform with delta cycle resolution for PV and PVT
- Synchronize with ISS execution
- Links with OSCI, Questa and other mixed-language simulators
- AVM Compliant

Benefits

- Facilitates C/C++ debug within hardware simulation context
- Eases SC and TLM adoption
- Empower SC testbench debug
- Faster debugging cycles with efficient object tracing
- Improves design understanding through HW and C++ code structure visualization
- No instrumentation for TLM tracing
- Intuitive to use
- Short setup time linking with users own make files and SC projects
- Build on Standards: GDB, gcc

TLM Debug Features

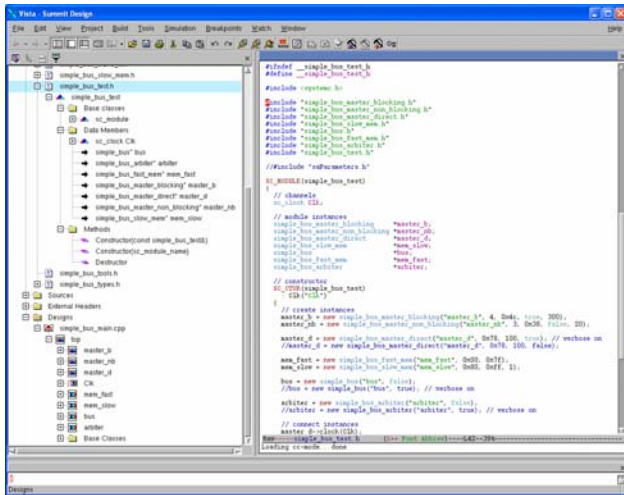
- Implicit transaction capture – no need for instrumentation
- Accurate flow of interface methods between masters and slaves
- Intuitive calling and return notation for suspended transactions
- Revolutionary *TLM Data Analyzer** surpasses waveform analysis techniques *Patent Pending



Intuitive TLM Viewer

Supports All Design Abstractions

- Abstract algorithm
- Un-timed behavioral description
- Transaction-level model
- Cycle accurate architecture



Tightly linked hardware design and C++ views

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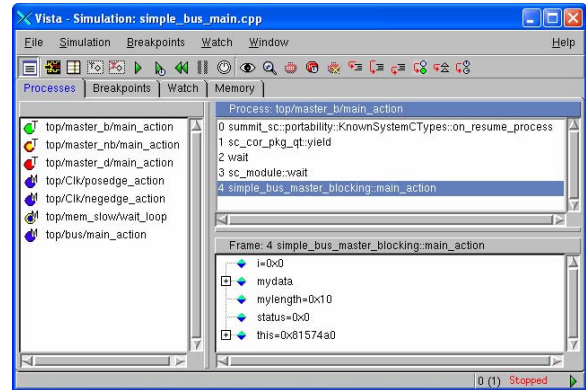
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SystemC Debug Features

Vista provides unique debug mechanisms such as runtime process activity browser with variable and stack tracing, waveform that can display any C/C++ object, and all the familiar debug operations including:

- Design threads listing and context switching
- Function call stack viewing and switching
- Break on time, source line, or process
- Object field value display in browser



Unique runtime process activity and stack browser

Link with ISS / SW Execution

Vista offers unique synchronization with ISS models allowing full visibility and control during ISS process execution. Vista also offers firmware tracing and debug during simulation.

Design Analysis

Vista links seamlessly with System Architect™ to provide system analysis and quantify performance metrics such as transactions throughput and latencies. Vista's unique variable tracing allows analyzing process states and attributes under various simulation scenarios.

Design Flow Integration

Vista easily integrates into your SC text-based file and project structures using "vista_cc" wrapper. Set up is very simple and short without any code modifications.

Vista can automatically generate a graphical library to use within the Visual Elite™ environment, enabling SystemC IP to be directly connected to HDL components and co-simulated with a variety of supported commercial mixed-language simulators such as Questa™.