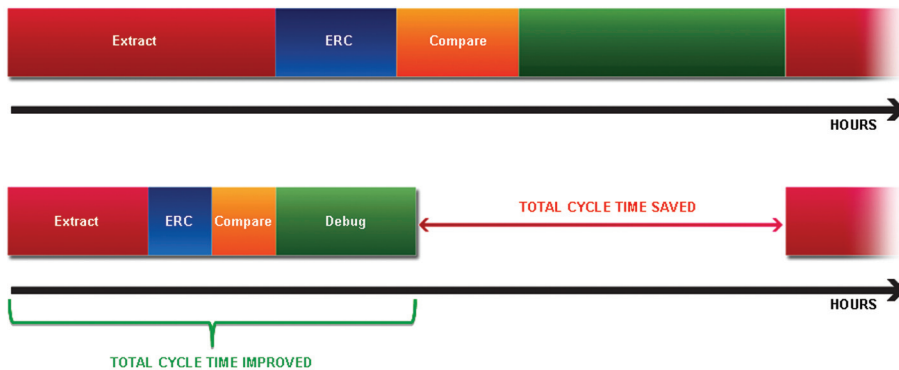


Calibre nmLVS

D A T A S H E E T



Calibre® nmLVS is two to three times faster than traditional layout vs. schematic processes.

Calibre nmLVS: The Gold Standard

Foundries and integrated device manufacturers (IDMs) have proven the excellence of Calibre nmLVS through their unprecedented support of Calibre's device extraction, comparison, and debugging technology. Direct support of the Calibre rules by the foundries and IDMs provides comprehensive coverage for your process nodes, and you have access to the rules that ensure first-pass silicon success. Our strong relationship with your manufacturer makes the decision to use Calibre technology a low-risk choice.

Faster Cycle Time

Improved extraction for advanced stress parameters (especially at 45 nm and below), electrical rule checking capability, comparison that now takes only minutes, and an improved, easy to use debugging environment reduces the overall time spent in LVS. The ability to use hierarchical design and hardware scaling further reduces your verification time.

Complete LVS Verification Solution from 130 to 45 nm

Calibre nmLVS provides best-in-class device recognition and parameter extraction for source netlist comparison, and its robust and easy-to-use integration lets you insert Calibre nmLVS into your design flow, allowing you to use Calibre as a single platform for cell/block and full-chip verification.

Customers who are designing at the cutting edge of 45 nm can use Calibre to extract all the new advanced stress parameters that are required to do accurate modeling at that process node. At 45 nm, extracting advanced stress parameters, applying design-for-manufacturing checks, and performing electrical as well as topological design rule checks during the layout vs. schematic (LVS) process is a must. Calibre nmLVS makes this possible, saving you time and money.

Benefits of Ownership

- **Market Leadership** — Calibre nmLVS continues to lead the market. Preferred by engineers and management for its proven performance, capacity, reliability and debug ease-of-use.
- **Best-in-Class Accuracy** — Device recognition accuracy is crucial for tape-out success. Calibre nmLVS delivers the trusted device recognition accuracy and timely execution required for world-class silicon delivery.
- **Fast Runtime** — Automated proprietary hierarchical and logic injection technologies provide virtually unlimited design scope with fast runtimes. Multi-threaded and distributed CPU processing capabilities ensure future proof scaling on your hardware.
- **Flexibility** — Calibre nmLVS is ideally suited for processing any size job requiring intricate device parameter extraction, whether it's an analog/RF design or a multi-million gate IC.
- **Reliability** — With thousands of users, Calibre nmLVS sets the standard for reliability and predictability in all operations.
- **Design Debugging and Ease-of-Use** — Calibre nmLVS provides an intuitive and easy-to-use integrated design verification debugging environment to help you find and fix design issues.

Superior Device Extraction and Analysis

Both analog and digital device extraction require comprehensive and accurate device extraction capabilities. Calibre nmLVS provides automatic device recognition and parameter extraction for standard devices with typical BSIM3/4 and PSP parameters, as well as a user-defined option when more complex requirements are needed. In both cases, Calibre nmLVS can extract parameters using standard SVRF or TCL-based rules. See table for the required measurements that nmLVS provides.

Advanced Device Parameters

As transistor sizes continue to decrease, the complexity and number of parameters that are required for extraction are increasing. At 45 nm and below, foundries are extracting custom parameters that are important to their unique process. With the ability to create user-defined parameters for extraction, nmLVS is “future-proof” and ready for the unknown at 32 nm and below. Calibre nmLVS goes beyond where older generation LVS tools break down at 45 nm because they cannot extract parameters involving more than one transistor.

Comprehensive Debugging

Time spent in debugging can dramatically affect time to tape-out, but incomplete debugging can result in yield failures. Calibre nmLVS provides a thorough scope of debugging and analysis functionality integrated into a user-friendly environment that helps you find and fix layout vs. schematic issues quickly and effectively. Full cross-probing of SPICE netlists, with browser and netlist comparison, is available, as is identification of shorts and isolation.

The graphical environment is easy to use and includes design-fix suggestions and visual indication of the location of geometrical and electrical violations, such as shorts in the layout. A dynamic results-viewing environment allows you to see violations and start fixing them as soon as they are detected, rather than waiting until the DRC run completes.

Electrical Rule Checking

Calibre nmLVS can be used with rule decks containing electrical rule checks to find design errors not identified by traditional tools. For example, you can identify and correct errant

| Process Node | Required Measurements |
|--------------|---|
| 180–150 nm | W, L, AS, AD, PD, PS (BSIM3) |
| 130 nm | SA, SB (BSIM4/PSP) |
| 90–65 nm | SCA, SCB (BSIM4/PSP) |
| 45 nm | Active spacing, poly spacing, custom measurements |
| 32 nm | Finfet support nmLVS is ready for new, custom measurements |

signal paths, well connection errors, or other soft connection errors. Running multiple electrical rule checks independently or together, Calibre nmLVS allows you to use standard rules or to create custom rules as needed. You can develop design checks that can be used to look for ESD violations that are becoming more complex at advanced nodes. This capability is not available from any other tool today. With Calibre nmLVS, you can achieve greater verification of your designs and be assured of reducing the number of die that are susceptible to electrical failures.

Fully Scalable Solution

Calibre nmLVS allows you to maximize your resources and minimize the time to complete verification by taking advantage of design hierarchy and using hardware scaling on local and remote machines.

Hierarchical Design Methodology

Calibre nmLVS reduces your turn-around time for IC verification with a logic injection technology that automatically scans for repeated and common device patterns. By recognizing repeated hierarchy in your design, Calibre nmLVS can simplify the repeated devices and “inject” a level of hierarchy it then uses during the comparison process.

Hardware Scaling

Calibre nmLVS also enables MT, MTFlex, and Hyperscaling to maximize hardware and software resource use. Multiple technologies that can scale for efficient and effective use of your hardware and allow for growth is one of the many benefits of the Calibre platform.

Platforms Supported

32 and 64 bit Linux Redhat, SUN Solaris

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