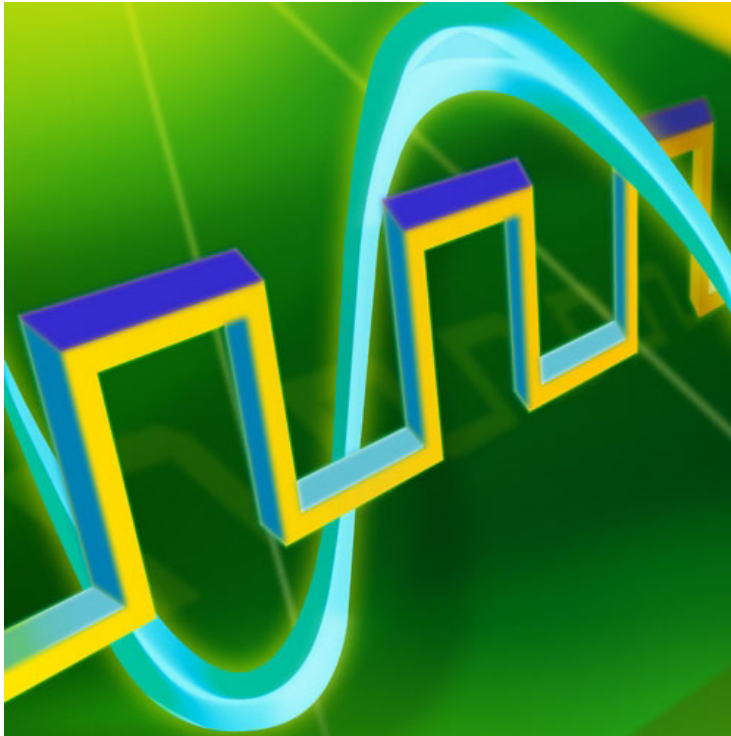


# ADVance MS

D A T A S H E E T



*ADVance MS is a language-neutral, mixed-signal simulator that enables top-down design and bottom-up verification of multi-million gate analog/mixed-signal System-on-Chip designs.*

## ADVance MS Simulator Provides Comprehensive Environment for Analog/Mixed-Signal Designers

The Mentor Graphics ADVance MS™ (ADMS) simulator gives designers a comprehensive environment for verifying complex analog/mixed-signal (AMS) System-on-Chip (SoC) designs. ADMS combines four high performance simulation engines in one efficient tool: Eldo™ for analog large-signal and frequency domain simulations, ModelSim® for digital simulations, Mach™ for fast transistor-level simulations and Eldo-RF™ for modulated steady state simulation.

ADMS is fully integrated with the Mentor Graphics Design Architect-IC™ (DA-IC) tool, the Cadence® Analog Design Environment, and the ModelSim graphical interface. The CommLib™ QuickStart™ library of essential telecommunication blocks jumpstarts your development of system level designs and exploration of architectural variations. The TCL scripting language enables batch control of the simulation.

### Major product features:

- Single kernel solution and optimization techniques for fast, accurate mixed-signal simulation
- Four high-performance, customer-proven simulation engines: Eldo for analog, ModelSim for digital, Mach for transistor-level, and Eldo-RF for modulated steady state simulation
- Complete language support includes VHDL, Verilog, VHDL-AMS, Verilog-AMS, SPICE, and C
- Integrated into the Mentor Graphics AMS SoC Design flow and Cadence Analog Design Environment
- CommLib QuickStart library of parameterized, mixed-signal behavioral models can be customized and extended

### Major product benefits:

- Enables top-down design and bottom-up verification of multi-million gate AMS SoC designs
- Lets designers choose their own language and simulation algorithm combinations
- Saves time and boosts productivity by combining proven, industry-leading simulation technologies, and supporting a variety of languages
- Builds on previous design investments through its design flow integration with Mentor Graphics Design Architect-IC and Cadence Analog Design Environment
- Empowers high-level, system-level design, architectural exploration, and rapid learning of behavioral modeling techniques

## Meeting the Mixed Signal Challenge

Analog/mixed-signal SoC designs combine analog and digital content more tightly than ever before. They increasingly depend on integrated analog blocks such as A/D and D/A converters, phase-locked loops, and adaptive filters. This increased level of integration puts tremendous pressure on designers. Traditional design tool flows force designers to develop analog and digital subsystems in isolation, delaying the integration of these components until IC layout, and the testing until after fabrication. As a result, AMS SoC design has become a slow, expensive and error-prone process. AMS SoC designers need the same kind of tool integration that digital designers already enjoy — hardware description languages (HDLs) and behavioral models that automate the design process. This is the level of automation that ADMS provides.

## Optimize Your Simulation Strategy

### The Efficiency of a Single Kernel Architecture

The ADMS single-kernel architecture eliminates IPC/backplane overhead while providing a unified simulation cycle and a single all-inclusive database. Designers can freely combine VHDL, Verilog, VHDL-AMS, Verilog-AMS, SPICE, and C anywhere in their designs because ADMS is language-neutral and uses a single netlist hierarchy.

### The Power of Multiple Engines

Gain all the advantages of digital, analog and mixed-signal standard HDLs and SPICE in a single simulation environment. ADMS brings together the simulation engines from ModelSim, the industry-leading digital VHDL/Verilog simulator; Eldo, a popular general-purpose analog simulator; Mach, a high-speed transistor-level simulator for timing, and Eldo RF for specialized RF design challenges. Use the HDL source models and supporting packages in the CommLib QuickStart library to speedup communications and multimedia applications.

### The Advantage of Uncompromising Performance

Gain access to all Eldo primitives and optimized standard Eldo IC device models including BSIM3, BSIM4, VBIC, and HICUM. Easily perform transient, DC, AC and noise analysis. The unique ADMS architecture ensures a fast, accurate simulation of complex analog and mixed signal designs at any level of abstraction.

### The Fast Solutions

Circuits can be described and simulated at any level from behavioral to the device level, whether incorporating digital, analog or mixed-signal elements. Digital parts simulated by ModelSim can be used in ADMS without any modification. SPICE sub-circuits can be used anywhere in the design hierarchy for greater flexibility in modeling. HSPICE compatible SPICE models work without modification. There are close foundry links through popular device models and design kits — from system to silicon.

### Easy to Learn and Use

The ADMS interactive GUI is based on the popular ModelSim interface. It adds a versatile viewer that displays digital logical levels and analog voltages and currents. ADMS can be used stand-alone or integrated into two popular schematic driven environments. These integrations protect previous tool investments while enhancing their capabilities.



*The Cadence flow features the same look and feel as any simulator inside Analog Artist, but gives designers access to all the analysis commands and options of industry leading Mentor Graphics Eldo.*

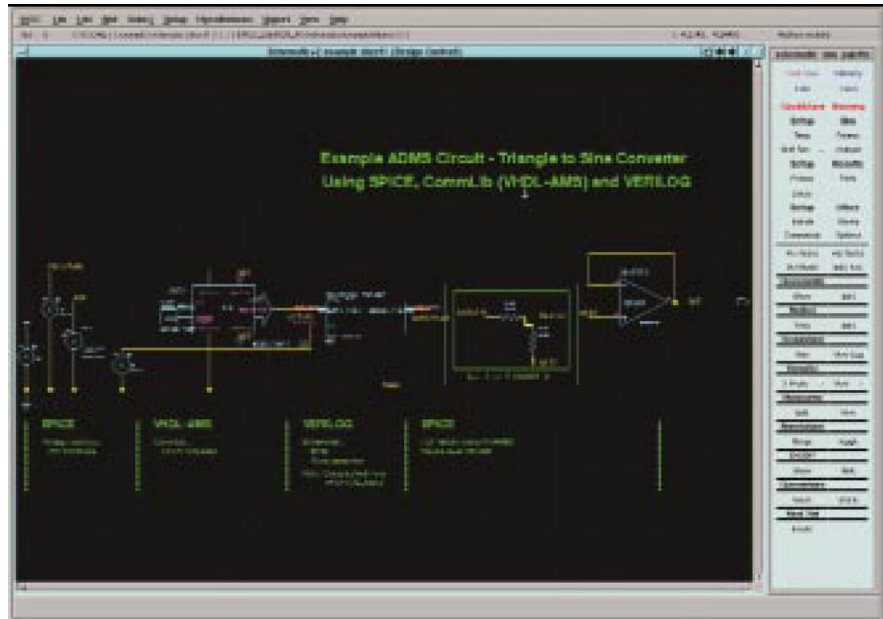
## Mentor Graphics Custom IC Design Flow

The custom IC design flow from Mentor Graphics features Design Architect-IC, a powerful tool for design entry.

Mentor tightly integrates ADMS and Design Architect-IC by combining advanced model registration and selection with the DA-IC simulation cockpit and EldoNet™ — Mentor's high-speed hierarchical netlisting application. This flow features fast data entry, rapid creation of function blocks for top-down design, and powerful data modeling. Design Architect IC is quick and easy to learn and integrates seamlessly with the other tools in Mentor's custom IC design flow.

### Cadence Flow

ADMS integrates into the Cadence Analog Design Environment. This achieves the same look and feel as any simulator inside the environment, but gives designers the advantage of ADMS analysis, commands, and options. An enhanced symbol library providing specific Eldo devices is compatible with the Cadence library. ADMS is the only way to get mixed-language simulation in the Cadence environment without the backplane overhead.

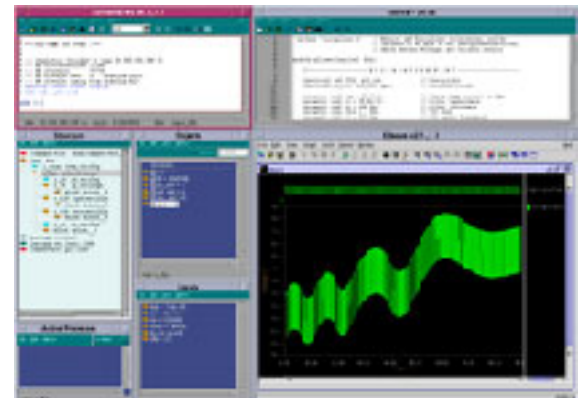


*Mentor Graphics Design Architect-IC flow features fast data entry, rapid creation of functional blocks, and powerful data modeling.*

### ADMS Stand-Alone ModelSim Flow

ADMS also offers a fully featured, stand-alone flow based on the ModelSim graphical interface. Mentor extends the familiar interface with menus, function and displays for integrated mixed signal model development. Dynamically linked debugging windows help to pinpoint problems. The structure window provides a hierarchical view of the design. The source window allows viewing and editing of VHDL-AMS source code. The objects window displays names and values of signals and quantities of the region on display. The locals window displays names and values of the selected process. The active process window shows lists of processes identified by their pathname.

The Ezwave window displays the simulation results within a graphical waveform viewer and signal post-processor.



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## CommLib QuickStart

A key component of the ADMS environment is the CommLib QuickStart library of essential behavioral models and supporting packages for communications applications. Each model describes the characteristic functionality of the corresponding device class using abstract modeling techniques.

### Speeds Up System Design and Evaluation

CommLib QuickStart HDL source models and supporting packages act as an extension to the ADMS simulator. They make it easy to apply efficient, top-down development techniques to AMS SoC designs. QuickStart models provide abstract blocks to speed up system level design and encourage architectural exploration. They mix freely with SPICE macromodels, subcircuits, and primitives and other VHDL-AMS and Verilog-AMS models. You can fine-tune them by defining input parameters to match system design specifications. This allows designers to quickly build working examples.

### Provides a Key Learning Tool

Having clear source code examples of parameterized models takes some of the mystery out of design. CommLib QuickStart examples provide valuable lessons in behavioral modeling techniques. They can make it much easier when adopting existing models or designing your own.

### Supplies Customizable Source Code

The source code can also serve as prototypes for new models. You can customize and extend the models to fit special requirements or to model more complex functions.

### Introduces the Full CommLib Library

To accelerate simulation and verification, progressively more detailed versions, including secondary and tertiary effects, can be drawn directly from the optional CommLib library. For even more complex applications or rapid turnaround situations, Mentor Graphics Consulting offers complete support.

## Top-Down AMS Design

Consider what's needed for effective support of your AMS SoC design challenge.

### System Level

Efficient IC design flow begins with architectural and algorithmic investigations using C, Matlab, paper designs and HDLs. System level designers create abstract models within ADMS of each top-level module, using RTL for digital blocks and abstract analog models for analog blocks. The QuickStart library of basic models helps them get started and allows designers to rapidly build working examples.

### Detail Level

The system level team can then use ADMS to pass the design down to the detail teams as a “working” specification in a form that the teams can use and in languages that the teams can understand. The language neutral

capabilities of ADMS facilitate global partnerships and outsourcing. The original language of the system design or the IP models won't hold back development.

### Transistor Register Level

While the digital design team works toward synthesis, the analog team's goal is a transistor-level design. The QuickStart library becomes an educational resource of behavioral modeling techniques. Models can be customized and extended by the user, or more complex versions can be drawn from the hundreds of parameterized models in the optional CommLib model library. The detailed designers use ADMS to decompose the system design into larger and larger numbers of blocks containing more and more detail, until the design has been verified at the most detailed level. At each step, the design is carefully compared to its previous step to assure that requirements are met throughout the process. When the blocks contain the necessary detail, the analog engineer uses ADMS to convert each block to the transistor level.

## Bottom-Up AMS Verification

Behavioral models continue to play a crucial role in bottom-up AMS SoC verification. Each block must meet its specification. Digital blocks are correct by construction. Analog blocks, however, require testing of implementation-specific vulnerabilities in addition to functional testing, a task made easier by ADMS.

### Model Construction

ADMS allows the use of abstract analog models that exhibit the same

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characteristics as the transistor level blocks. Basic models can be extended from the built-in QuickStart library or taken directly from the many levels of telecommunications and multi-media models available in the optional CommLib library. Accuracy of these hundreds of parameterized AMS models can be fine-tuned through the CommLib BMC™ (Behavioral Model Calibration) function. This allows you to calibrate your models to precisely match the behavior of actual circuits at the transistor level, ensuring accurate simulation and verification. CommLib abstract models simulate ten to one thousand times faster than the original blocks.

### Model Verification

In checkerboard verification, only the block currently being converted to the transistor level needs to be simulated at the transistor level. The remainder of the circuit continues to be simulated with behavioral models, RTL or abstracted blocks. With ADMS, the team can achieve transistor level accuracy where needed, while running their simulation orders of magnitude faster than they could with traditional techniques.

### Design Verification

Once the blocks have been individually verified and their behavioral models finely calibrated, system verification continues with ADMS. Using the abstracted models, the team can invoke massive simulations involving mega-vectors, multiple seconds of simulated time, and many corner cases. The result is fast and thorough design verification before the expense of fabrication.

### Summary

Mentor Graphics' ADMS is a superior tool for the development and verification of complex AMS SoC designs. It delivers the speed, versatility and accuracy necessary to automate the mixed-signal design process. It also delivers the effective control necessary for true top-down design and bottom-up verification. Since ADMS is a language-neutral and integrates with popular design environments, it protects previous design work while letting designers take full advantage of the most powerful and effective design and verification tool available today.

Visit our web site at [www.mentor.com/dsm](http://www.mentor.com/dsm) for the latest product news.

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