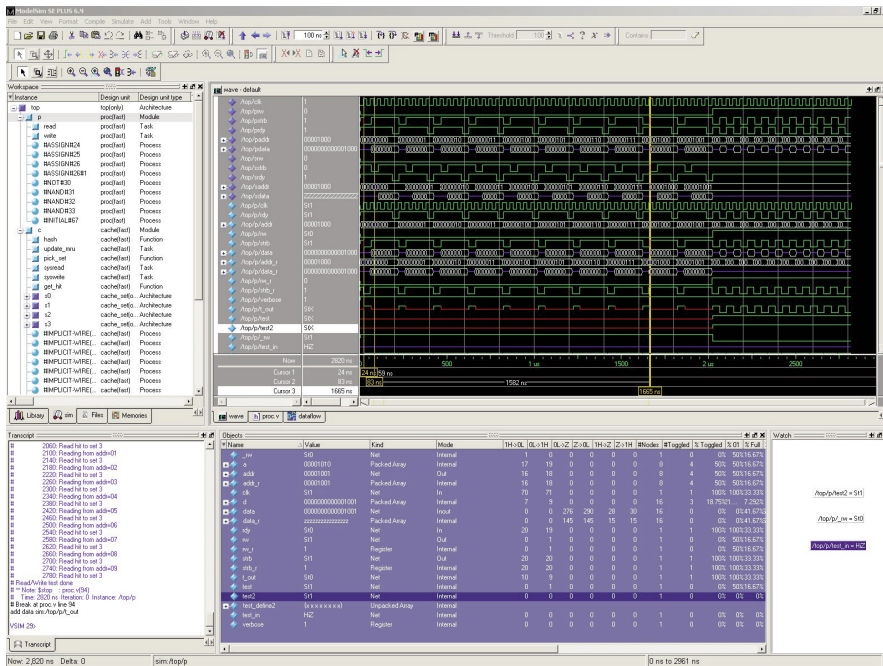


# ModelSim



## Major product features:

- Leading RTL and gate performance with ASIC sign-off
- Native support of VHDL, Verilog, SystemVerilog, and SystemC
- Powerful, intuitive GUI speeds RTL and gate debug
- Textual and graphical dataflow with automated X-tracing and source annotation
- Code coverage
- Post-simulation debug
- Customizable, open architecture with C and Tcl/Tk
- Integrated JobSpy for simulation farm support
- Upgradeable to Questa for advanced verification solutions

*ModelSim provides scalable HDL simulation solutions for a broad range of design sizes and complexities.*

## Leader in Single Kernel, Mixed Language Technology

Mentor Graphics® was the first to combine single kernel simulator (SKS) technology with a unified debug environment for Verilog, SystemVerilog, VHDL, and SystemC.

The combination of industry-leading performance and capacity with the best integrated debug and analysis environment make ModelSim the simulator of choice for both ASIC and FPGA design. The best standards and platform support in the industry make it easy to adopt in the majority of process and tool flows.

## High-Performance, Scalable Simulation Environment

ModelSim provides seamless, scalable performance and capabilities. Through the use of a single compiler and library system for all ModelSim configurations, employing the right ModelSim configuration for project needs is as simple as pointing your environment to the appropriate installation directory.

ModelSim PE and LE enable individual engineers to develop and debug small to medium size design blocks on Windows and Linux, respectively. ModelSim SE combines high performance and high capacity with the code coverage and debugging capabilities required to simulate larger blocks and systems and attain ASIC gate-level sign-off. ModelSim SE offers the ability to simulate very large designs through support of 32 and 64 bit UNIX and Linux and 32 bit Windows®-based platforms.

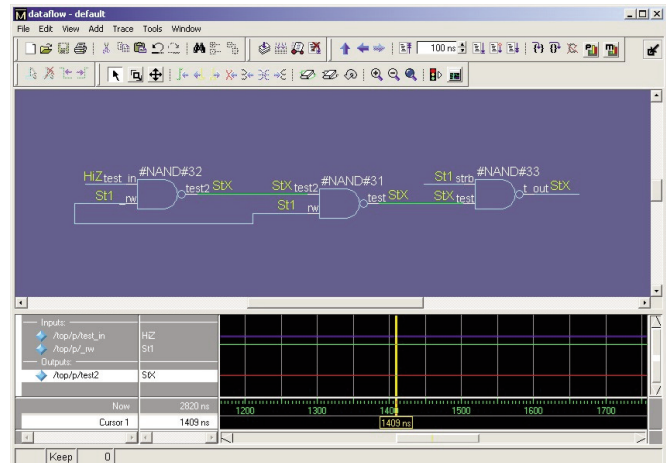
The ModelSim SE *vopt* usage mode achieves industry-leading performance and capacity through very aggressive, global compile and simulation optimization algorithms of Verilog and VHDL. The *vopt* performance mode can improve Verilog and mixed VHDL/Verilog RTL simulation performance by up to 10X. The *vopt* mode can also improve gate-level performance by up to 4X and capacity by over 2X.

ModelSim also supports very fast time-to-next-simulation turnarounds while maintaining high performance with its new black box use model, known as *bbox*. With *bbox*, non-changing elements can be compiled and optimized once and reused when running a modified version of the testbench. *bbox* delivers dramatic throughput improvements of up to 3X when running a large suite of testcases.

### Easy-to-Use Simulation Environment

An intelligently engineered graphical user interface (GUI) efficiently displays design data for analysis and debug. The default configuration of windows and information is designed to meet the needs of most users. However, the flexibility of the ModelSim SE GUI allows users to easily customize it to their preferences. The result is a feature-rich GUI that is easy to use and quickly mastered.

A message viewer enables simulation messages to be logged to the ModelSim results file in addition to the standard transcript file. The



*ModelSim SE native support of SystemVerilog design constructs enables high-level design modeling and debug.*

GUI's organizational and filtering capabilities allow design and simulation information to be quickly reduced to focus on areas of interest, such as possible causes of design bugs.

ModelSim SE allows many debug and analysis capabilities to be employed post-simulation on saved results, as well as during live simulation runs. For example, the coverage viewer analyzes and annotates source code with code coverage results, including FSM state and transition, statement, expression, branch, and toggle coverage. Signal values can be annotated in the source window and viewed in the waveform viewer. Race conditions, delta, and event activity can be analyzed in the list and wave windows. User-defined enumeration values can be easily defined for quicker understanding of simulation results. For improved debug productivity, ModelSim also has graphical and textual dataflow capabilities.

The memory window identifies memories in the design and accommodates flexible viewing and modification of the memory contents. Powerful search, fill, load, and save functionalities are supported. The memory window allows memories to be pre-loaded with specific or randomly generated values, saving the time-consuming step

of initializing sections of the simulation merely to load memories. All functions are available via the command line, so they can be used in scripting.

## Graphical Usage Profiler

The profiler provides an interactive graphical representation of both memory and CPU usage on a per instance basis. It shows which part of the design is consuming CPU or memory resources, allowing engineers to more quickly find problem areas in their code.

## Advanced Code Coverage

The ModelSim advanced code coverage capabilities deliver high performance with ease of use. Most simulation optimizations remain enabled with code coverage. Code coverage metrics can be reported by-instance or by-design unit, providing flexibility in managing coverage data. All coverage information is now stored in the Unified Coverage DataBase (UCDB), which is used to collect and manage all coverage information in one highly efficient database. Coverage utilities that analyze code coverage data, such as merging and test ranking, are available. Coverage results can be viewed interactively, post-simulation, or after a merge of multiple simulation runs.

The coverage types supported include:

- *Statement coverage*: number of statements executed during a run
- *Branch coverage*: expressions and case statements that affect the control flow of the HDL execution
- *Condition coverage*: breaks down the condition on a branch into elements that make the result true or false

- *Expression coverage*: the same as condition coverage, but covers concurrent signal assignments instead of branch decisions
- *Focused expression coverage*: presents expression coverage data in a manner that accounts for each independent input to the expression in determining coverage results
- *Enhanced toggle coverage*: in default mode, counts low-to-high and high-to-low transitions; in extended mode, counts transitions to and from X
- *Finite State Machine coverage*: state and state transition coverage

## JobSpy

With integrated support of standard load sharing software, JobSpy provides the ability to easily manage and interact with simulation batch jobs. The JobSpy interface allows users to select any submitted batch job, monitor its status, or submit commands; such as, save a snapshot of a waveform, query simulation time, or suspend the job. This can be accomplished with the easy-to-use graphical interface or via the command line interface.

## Complete Product Support and Maintenance

Mentor Graphics provides the highest level of support in the industry through its unique Engineer of the Week approach. Customers receive support from the engineers who design the ModelSim products. A standard annual maintenance contract provides technical support, maintenance releases, the Informant email newsletter, and access to on-line support and technical services.

Visit our web site at [www.mentor.com/fv](http://www.mentor.com/fv) for the latest product news.

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