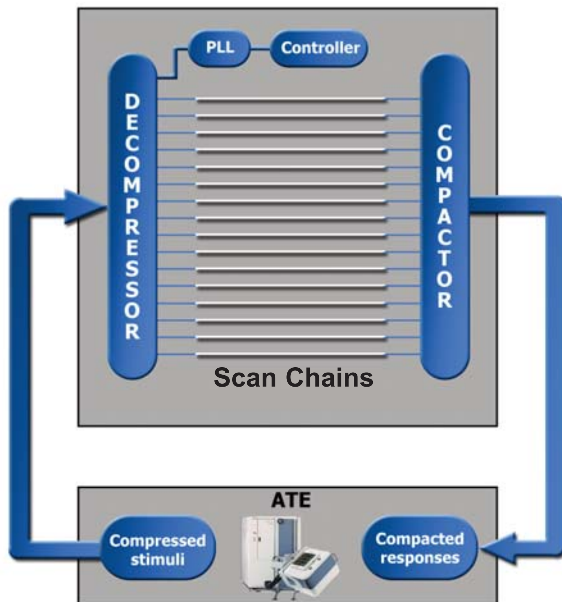
TestKompress

Design-for-Test

ATPG WITH EMBEDDED COMPRESSION

D A T A S H E E T



TestKompress uses the patented EDT technique to get the highest level of test quality while getting up to 100X pattern compression

High Quality Devices Delivered with Scan Testing

Creating high quality integrated circuits can only be achieved by employing high-quality production tests that identify manufacturing defects before they leave the factory. Shrinking geometries have introduced a wide variety of defect types that can only be detected with thorough scan testing. However, scan testing can be prohibitively expensive without high levels of pattern compression.

TestKompress® is the industry leading automatic test pattern generation (ATPG) tool that provides the highest quality scan test with the absolute lowest test cost. TestKompress has an industry-proven ATPG engine that applies effective fault models to your entire logic design. Manufacturing test costs are held in check by an award-winning test pattern compression technique called Embedded Deterministic Test (EDT™).

TestKompress has all the tools to configure a design with scan test structures into one that utilizes test pattern compression. Then the ATPG engine creates a compact set of compressed patterns that are ready to be applied by the automatic test equipment (ATE).

Comprehensive Scan Testing Techniques

Structural testing achieved through scan is one of the most effective manufacturing test methods for digital logic. Industry-proven fault models are used to uncover the most subtle defects. TestKompress supports standard “stuck-at” fault models for targeting static failures, and at-speed fault models for uncovering dynamically activated defects. It supports the use of on-chip PLLs for delivering accurate at-speed clock edges and both “launch off shift” and “launch off capture” transition fault application.

Effective and reliable at-speed test (e.g. transition and path delay fault models) requires that ATPG tools handle unknown states also referred to as X states. The patented X masking capability in TestKompress provides X tolerance and maintains high test coverage. The major sources of these X states during at-speed test are false and multicycle paths. The X

High Test Quality

- Thorough testing of digital logic with scan-based patterns
- Lower DPM with transition and path delay testing
- Consistent coverage achieved through robust “X” handling

Test Cost Reduction

- Reduces both ATE test time and test data volume by up to 100X
- Supports low pin count test strategies (as few as 1 scan channel)
- Flexible design flow supports any synthesis tool or strategy

Rapid Test Development

- Fast pattern generation through high performance ATPG algorithms
- Scalable performance with distributed processing
- Quick troubleshooting utilizing a friendly scan debugging environment
- ATPG Expert™ feature automates optimal results

Award-Winning Technology

- 2001 Product of the Year
- 2002 Best-in-Test
- 2006 IEEE Donald O. Pederson Best Paper

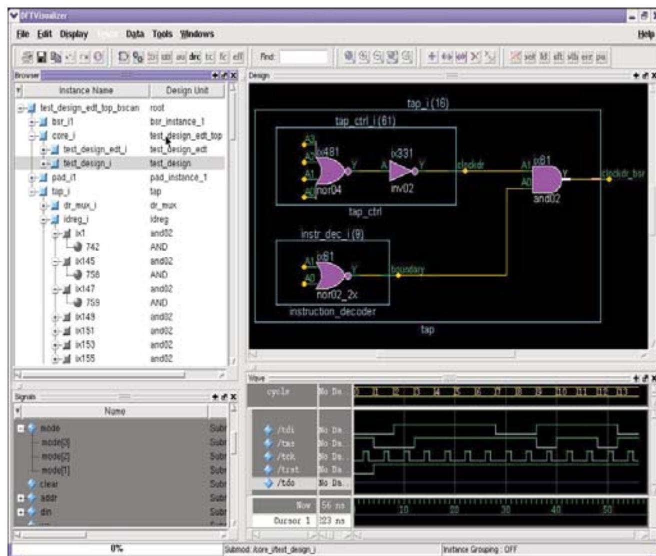
masking intelligently handles these paths by directly reading the SDC file. The result is higher test coverage, higher levels of compression and stable patterns on the ATE. Named capture procedures (NCP) provide a powerful means of supporting the generation of accurate at-speed clock pulses with the on-chip PLL. TestKompress also provides effective control of clock-gaters to maximize coverage.

In addition to the standard stuck-at faults and at-speed defects, TestKompress can also specifically target bridge defects. Bridging faults resulting from random particles can be targeted with an “N-detect” fault model. Feature dependent bridge defects can be targeted using a physical bridge fault model, with candidates extracted directly from the physical layout using Calibre® LVS.

Test Pattern Compression

TestKompress uses a patented technique called EDT to provide effective test pattern compression. Up to 100X reduction in both test time and pattern volume can be achieved without any loss in coverage. From the ATE standpoint, these compressed patterns operate the same as uncompressed patterns, except for the smaller tester memory footprint and faster test time. Patterns can be saved in a variety of formats including WGL and STIL.

TestKompress can use as few as a single scan channel to ease routing and external I/O concerns. Both the decompressor and compactor (the main components of the EDT logic) are part of the scan path so functional timing closure is not impacted. Area



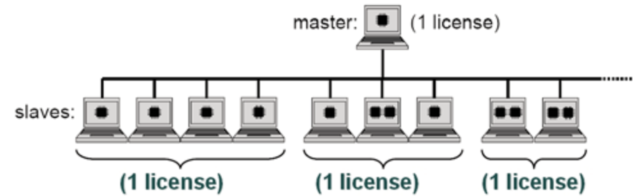
TestKompress’ DFTVisualizer is a powerful debug environment that includes a hierarchy browser, schematic viewer and waveform window

overhead is typically less than 1%. TestKompress doesn’t require any additional design changes such as test points.

The EDT logic in TestKompress can be generated in a number of different flows and is synthesis tool independent. The EDT logic can be added to the top level of a design or used in a modular configuration, placing a decompressor and compactor in each block of the design.

Getting Patterns Fast

The runtime performance of TestKompress scales with increasing



Distribution of ATPG is performed with ATPG Accelerator without the need for any special licensing

design complexity. It uses core ATPG algorithms that have been optimized for fast pattern generation without any loss in coverage or increase in pattern count. Optimal results are easily achieved by using the ATPG Expert capability. Further, TestKompress includes ATPG Accelerator™—an efficient system that distributes the ATPG run across multiple processors. Identical patterns are generated regardless of the number of processes employed. Robust fault tolerance ensures reliable results and consistent performance improvement. ATPG Accelerator requires no special licensing. Each incremental license of TestKompress enables up to four additional slave processes.

A comprehensive set of design rule checks (DRCs) ensures successful pattern generation. Debugging DRC violations and improving coverage is fast and easy with the DFTVisualizer™ debug environment. Schematic tracing and hierarchy browsing features intuitively display DRC and coverage information to help the user quickly resolve problems. Pattern verification is achieved by simulating the automatically generated testbench.

Failure Diagnosis

For those devices that fail scan test, TestKompress includes a powerful failure diagnosis engine that helps the user pinpoint where and how it occurred. It even works directly with failure logs from compressed patterns, thereby eliminating the need for special bypass patterns.

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