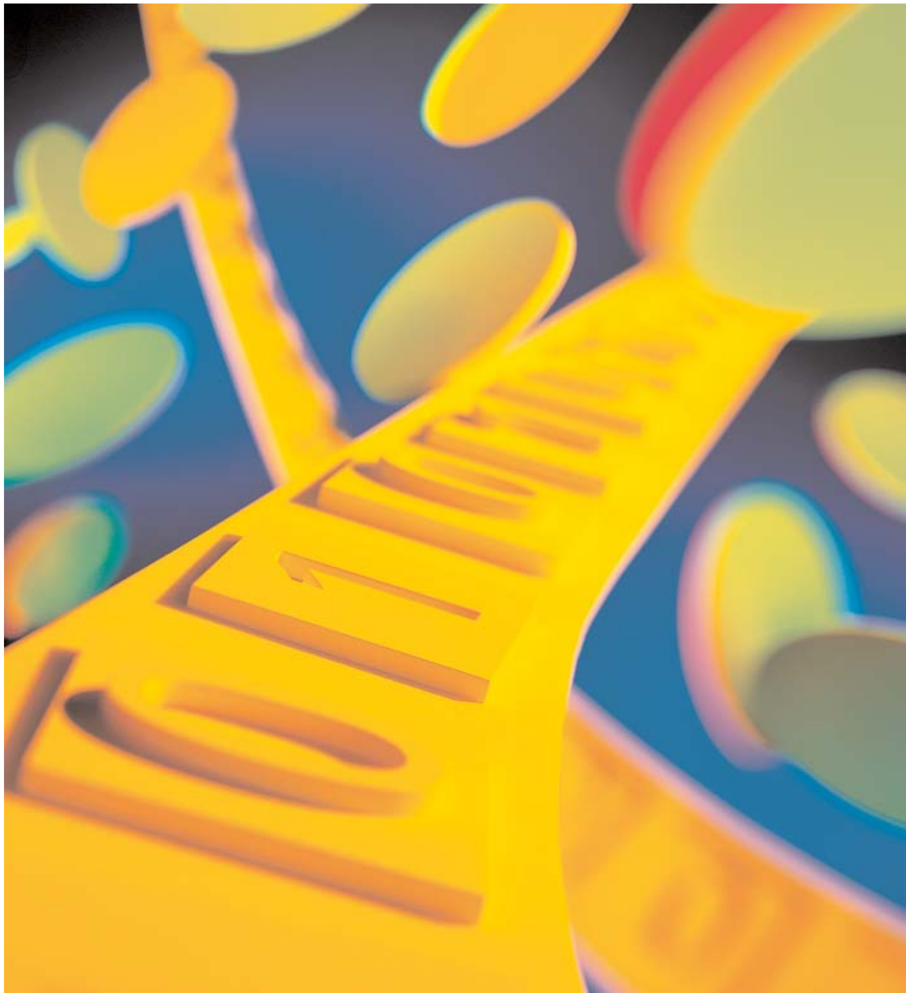
FASTSCAN

AND THE ATPG PRODUCT FAMILY

Design-for-Test

DATASHEET



FastScan has led the industry, setting the standard for ATPG products for more than a decade.

INDUSTRY-LEADING ATPG

Since structural test began replacing functional test techniques in the early 1990s, FastScan™ has led the industry as the most powerful automatic test pattern generation (ATPG) tool available.

As designs grow in complexity and shrink in feature size, additional test challenges emerge. FastScan meets these challenges and sets the standard for the highest quality and the most efficient test sets for today's designs.

COMPREHENSIVE FEATURE SET

FastScan is a powerful, yet simple tool. For the occasional user, FastScan offers every feature needed to generate high coverage, compact test sets quickly, with just a single command

For the power user, FastScan has been proven to offer the flexibility and features needed to deliver exceptional results on the most complex multi-million gate designs.

PERFORMANCE

- Highest performance ATPG for full and structured-partial scan designs
- Innovative compression techniques generate compact test sets in the shortest run times
- Distributed ATPG for dramatic reduction of runtime and no impact to coverage or pattern count

QUALITY

- Extensive fault model support, including stuck-at, IDDQ, transition, path delay and bridge
- On chip PLL support for accurate at-speed test
- False and multi-cycle support for fewest number of Xs and higher coverage
- FastScan MacroTest to automatically test small embedded memories and cores, including support of at-speed tests

TIME-TO-MARKET

- Comprehensive design rules checking to identify testability problems early
- Automatic simulation mismatch debugging reduces test validation time

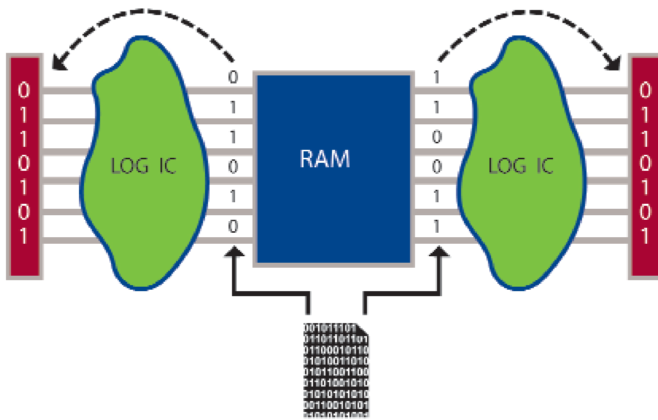
DESIGN FLOW

- Supported within industry-leading design flows for shorter time to market
- Integrated within the Mentor Graphics DFT tool suite to ensure automated, whole chip test

With its wide range of fault models, comprehensive design rules checks, extensive clocking support, and innovative algorithms for performance-oriented pattern compaction, FastScan leads the industry.

MEMORY AND MACRO TESTING

When a large number of small memories or register arrays are located throughout the design, FastScan's MacroTest capabilities offer a non-intrusive alternative to traditional memory built-in self-test (BIST). MacroTest converts block-based test vectors into scan patterns, saving time and effort in developing tests for these types of blocks. By using a design's existing scan circuitry, MacroTest adds no additional test logic and has no impact on performance. In addition, MacroTest patterns can be delivered "at-speed" to further improve test quality.



FastScan MacroTest creates tests for small embedded register arrays without adding additional memory test logic around the array.

AT-SPEED TESTING

As feature sizes move to 0.13 micron and below, the defect spectrum changes. More defects show up as speed-related failures and require detection through advanced test techniques. A comprehensive at-speed test solution is critical to ensure high-quality testing. FastScan's at-speed solution includes both transition and critical path testing.

Transition testing looks for delays on nodes at each gate, targeting the entire design for speed-related defects. FastScan's at-speed test solution can create both launch-off-shift as well as broadside transition patterns. FastScan CPA (critical path analysis) generates robust sequential patterns to detect defects along a design's critical paths. FastScan supports the use of on-chip PLLs for delivering accurate at-speed clock edges. With user input on the clocking procedures for the PLL, FastScan can generate accurate at-speed tests using the design's on-chip clocks.

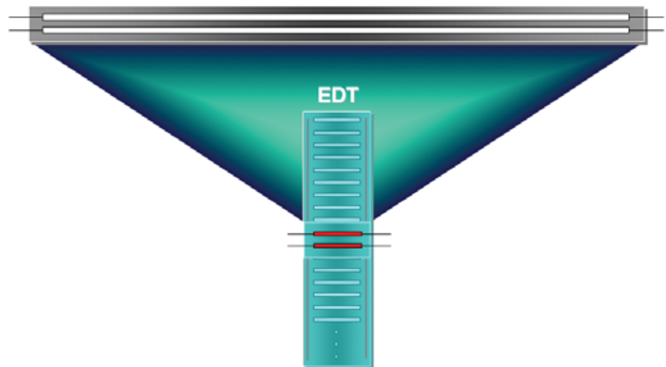
In addition, FastScan handles false and multiple paths in a smart way. It produces fewer number of Xs and higher coverage.

TEST SET COMPACTION

FastScan is known for delivering high-coverage, compact test sets. Recent innovations in the tool's algorithms have significantly enhanced compaction and performance even further.

However, with the growing need to improve test quality and with at-speed patterns becoming a standard, the amount of test data can still be an issue. In cases where test data volumes exceed automatic test equipment limits or vendor requirements, TestKompress® and embedded deterministic test (EDT™) offer a unique solution.

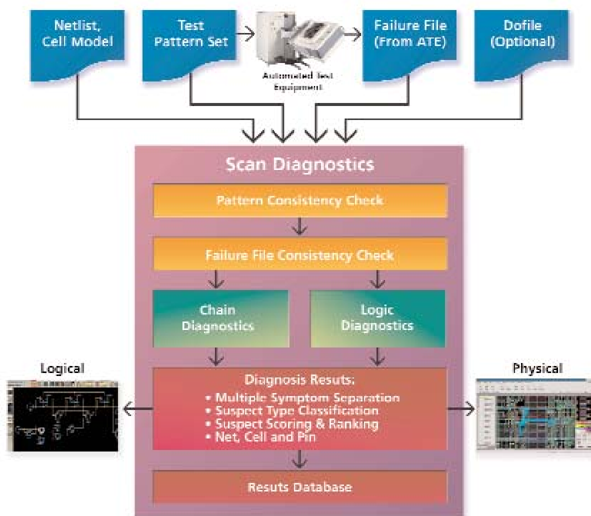
TestKompress uses the EDT technology to achieve dramatic and scalable test compression. TestKompress includes all the features of FastScan and delivers the same high-quality results. Thus, TestKompress is the natural transition from conventional ATPG to an ATPG-based embedded compression solution when test data volume becomes an issue.



Smaller geometries require at-speed testing to ensure high quality, while at-speed test accelerates the need for test compression to reduce the cost of achieving this quality.

DIAGNOSIS

Ramping up volume yield in a shortened product life is critical for nanometer designs. Failed devices need to be diagnosed to find out the route cause of failures so that correction and adjustment, such as design-for-manufacturing (DFM) recommendations can be reviewed. YieldAssist is a location-based scan diagnosis solution and it performs direct scan failure diagnosis of TestKompress or FastScan patterns. It helps customers quickly identify yield limiting defects and locates those defects in the physical layout. Results are linked to the Calibre physical verification viewing environment. For more information on YieldAssist, visit: www.mentor.com/dft



YieldAssist performs scan failure diagnosis of TestKompress or FastScan patterns, identifying and linking those defects in the physical layout.

OTHER SOLUTIONS IN THE ATPG PRODUCT FAMILY

Graphical Debug

Troubleshooting testability problems can be a difficult process – unless it's automated in a graphical environment like DFTInsight™. The graphical debugging environment simplifies analysis of testability problems. The tool generates a schematic view to display information, making it easier to isolate and correct testability problems. DFTInsight features include:

- Offers graphical analysis of testability rule violations to reduce testability debug time
- Displays pertinent schematic and simulation data to isolate and identify testability problems
- Displays a variety of user-selectable data and allows interactive design traversing for flexible design analysis
- Integrates with and supported by the Mentor Graphics FastScan, TestKompress, FlexTest™, DFTAdvisor™, and LBISTArchitect™ DFT tools

Design Complexity, SoCs, and Whole Chip Testing

The diverse design structures integrated onto a typical SoC design require various methods to ensure comprehensive testing. While high-quality, compact tests for a design's logic are important, it's just one part of a whole-chip test methodology.

FastScan and the ATPG product family are part of the Mentor Graphics technology-leading DFT tool suite, which includes integrated solutions for scan, ATPG, Test time/data compression, advanced memory test, logic BIST, boundary scan, diagnosis, and a variety of DFT-related flows. All Mentor DFT tools are available on UNIX and Linux platforms. For more information, visit www.mentor.com/dft.

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Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503-685-7000

Sales and Product Information
Phone: 800-547-3000
503-685-8000

Silicon Valley Headquarters
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, CA 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

North American Support Center
Phone: 800-547-4303

Mentor Graphics Europe
Mentor Graphics Corporation
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim Headquarters
Mentor Graphics (Taiwan)
Room 1603, 16F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-87252000
Fax: 886-2-27576027

Japan Headquarters
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3021

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