

MunEDA – WiCkeD Tools Overview

Introduction

Today's ASIC designs are facing ever more difficult challenges. With Market opportunity windows shortening, manufacturing costs increasing with shrinking geometry sizes, the financial and business risks of ASIC based products have increased substantially. Producing designs right the first time, or at least with the minimum possible number of re-spins, is a financial and business necessity.

These problems are further compounded for ASIC designs containing analogue circuitry. It is extremely challenging to design analogue circuits that are not only functional, but operate correctly across the required set of operating conditions and are as immune as possible to variations in the manufacturing process. It is commonplace for nominally functional designs to undergo multiple re-spins to reduce the sensitivity of the circuit to these variations and thereby increase the yield. High yields directly contribute to reducing the cost of high volume ASIC designs.

These issues today are typically addressed by analogue designers manipulating transistor parameters and predicting the outcome of these changes on the circuit performance using analogue simulation packages such as Spectre, Eldo and HSPICE. Unfortunately the number of parameters is usually large, often with complex interactions, resulting in a huge number of simulations that need to be run to assess how these changes would impact circuit performance. Because of these factors it can be a very lengthy and sometimes practically impossible task, to produce a design that is both functional and optimised for maximum yield.

[MunEDA](#) provides software for the analysis, performance enhancement, and yield optimization of analogue, mixed-signal and digital ASIC designs. The WiCkeD software suite enables customers to reduce analogue circuit design times and to maximize their robustness and yield. MunEDA's solutions are in industrial use by leading [semiconductor companies](#) in the areas of communication, computer, memories, automotive, and consumer electronics.

Step 1 – Circuit Preparation

Based on the chosen circuit schematic the first step of the WiCkeD™ sizing and design centering flow is the preparation of the circuit and testbenches in order that simulation, analysis and optimization can take place. The characteristics of a circuit at the transistor level depends on its topology, design parameters, process variation during production and operating conditions at the time of measurement. During Circuit Preparation the schematic is parameterized. All device geometry parameters intended to be optimized by WiCkeD™ are defined as design variables in the schematic cell view of the design framework environment using the initial values (if available) for optimization.

The goal is to find design parameter values that ensure as many manufactured circuits as possible fulfill their specifications in the full operating range. WiCkeD™ helps achieve this by providing the

designer with tools and methods for analysing and optimizing their circuit design.

The WiCkeD™ tools are fully integrated with leading analogue design frameworks such as Cadence Virtuoso & Mentor Graphics IC Studio. We also rely upon simulation tools such as Spectre, Eldo & HSPICE to perform the necessary simulations. All simulation results are stored in a database such that for a given set of parameters no simulation run need ever be repeated.

Step 2 – Parameter Setup

The number of sizing rules is usually too large to be set up manually for each transistor device. The WiCkeD™ automatically identifies basic circuit structures such as current mirrors and level shifters and assists the designer by automatically creating sizing rules for them. Sizing rules are used in WiCkeD™ for both circuit analysis and interactive and automatic sizing.

Step 3 - Feasibility Optimisation

Of the possible sets of all design parameters only a few satisfy all sizing rules. The restricted design space that satisfies all sizing rules is called the "feasible region". For many circuits, the feasible region is very small (perhaps 1% of the total design space), and it is sometimes difficult to find a set of design parameter values that satisfies all sizing rules.

WiCkeD™ will automatically modify design parameter values in order to find a feasible point in the design space. The user chooses between algorithms "find closest" and "find central". "Find closest" modifies design parameter values as little as necessary to fulfill the sizing rules. This is useful when a few rules are slightly violated, however the design is otherwise considered acceptable. "Find central" over-fulfills all sizing rules as far as possible. This approach is useful for quickly finding an initial sizing.

Step 4 - Nominal Optimisation - DFM

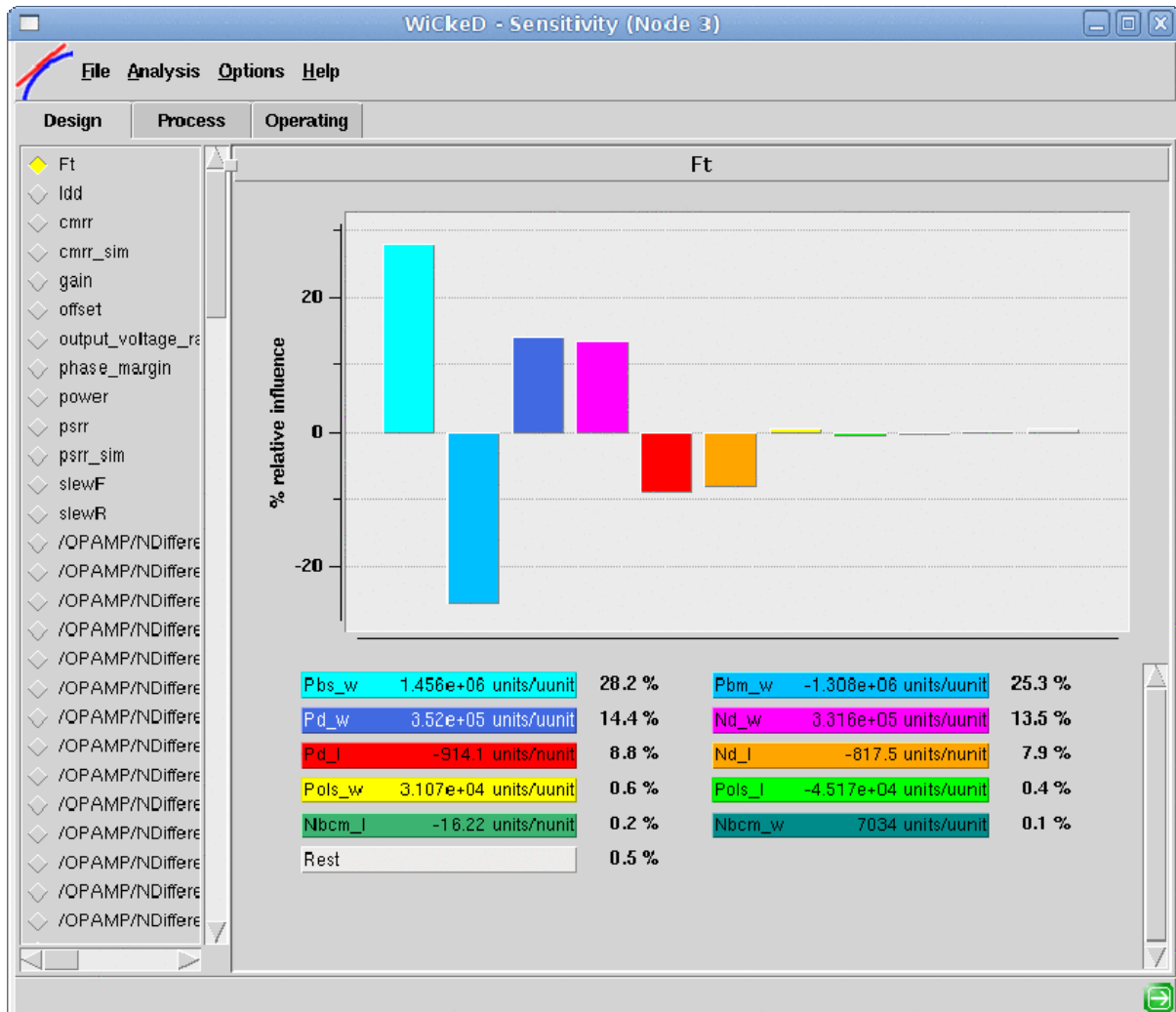
WiCkeD™ DFM Nominal Circuit Optimization provides three algorithms for automatic performance optimization. The designer enters performance specifications and selects parameters to be modified. Available algorithms are:

- Least-squares. Performance specifications are fulfilled, but the optimizer does not try to over-fulfill them
- Parameter distances. The optimizer tries to over-fulfill each specification as far as possible. Weight factors can be changed by the designer.
- Stochastic. Parameters are modified in a random manner over a sequence of generations with decreasing variance.

The first two optimizers are gradient-based. They converge quickly to the next local optimum of their goal function. Since the design space is restricted to the small feasible region, this is usually the only optimum. In rare cases with ill-defined, non-continuous performance functions over a large

design space with few constraints, the later two optimizers provide a global approach to optimization. For most practical circuits, gradient-based optimization outperforms global optimization regarding both algorithmic effort and quality of results.

WiCkED also has the ability to identify dependencies between specific transistors and circuit performance parameters. This capability informs designers of which transistors influence a particular performance parameter and the degree of that influence.



Step 5 - Design Centering - DFY

After determination of yield with WiCkED™ Monte-Carlo Analysis (able to handle full worst case operational parameter sets) the distribution of the performances as well as the parameter distances are measured and analysed. The next step is a Worst Case analysis and the calculation of the worst parameter distances used for Design Centering and Yield Optimization. The user can choose between an iterative optimization method or an automated yield optimization engine to increase the parametric yield to the desired maximum. Design is ready for Layout!

Summary

WiCkeD™ is a powerful suite of software tools for the analysis and optimisation of analogue circuits. It helps designers find solutions to complex design problems quickly, resulting in a significant reduction in design time and effort.

MunEDA's unique algorithms for automatic yield enhancement and circuit robustness can significantly improve the area and yield of analogue designs saving costly respins, reducing development costs and shortening time to market.

Wicked has been in production since 2002 and has been purchased by many of the world's top semiconductor companies like Samsung, Hynix, Infineon, STMicroelectronics, Qimonda, Faraday, ON Semiconductor, X-Fab and others.

Customer quotes:

Günter Kornmann, Director Analogue Mixed Signal Designflows, Infineon Technologies AG:

"WiCkeD is Infineons state of the art DFM-DFY tool in front-end design and fully integrated into Infineons Communication, Automotive and Memory Designflow. It is used since 2002 in more than 300 design and tape-out projects with Infineon in RF Design, High-Speed Analogue, High-Speed Digital, Automotive Power, Embedded Memory, Enhanced Digital Cell Library Modeling, and other applications."

Pierluigi Daglio, NVM AMS Flows & Methods Manager, STMicroelectronics:

"WiCkeD is a perfect tool for circuit analysis, design optimization and yield enhancement. STMicroelectronics has used WiCkeD based on Mentor Eldo circuit simulation in numerous benchmarks and real applications and proved it helps to design more robust circuits with a better yield."

Robert Bosch GmbH (From ANASTASIA report):

"Using the WiCkeD tools from MunEDA the designer undertakes a sequence of steps and methodologies that guide to a ready sized analogue circuit. Within these steps both the operation region (temperature, supply voltage) as well as the statistical process variations will be considered. Additionally the developer gets estimation about the expected yield. With the consequent use of these methods at least 2 redesigns per year can be saved. This leads to improved time-to-market and lower development costs."

Contact

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