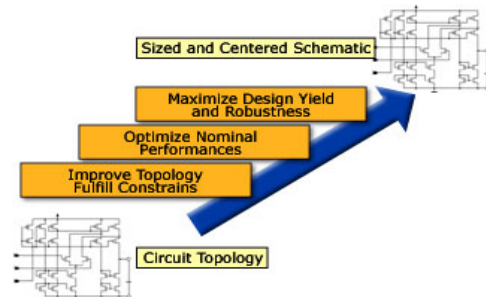
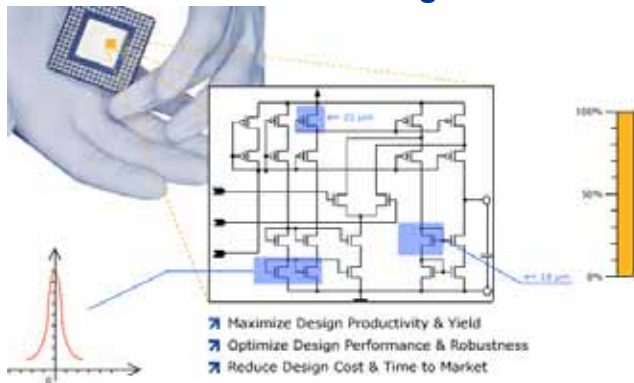



Product Overview

MunEDA provides leading EDA technology for analysis and optimization of yield and performance of analog, mixed-signal and digital designs. MunEDA's products and consulting enable customers to reduce the design times of their circuits and to maximize robustness and yield. MunEDA's solutions are in industrial use by leading semiconductor companies in the areas of communication, computer, memories, automotive, and consumer electronics.

MunEDA Design for Manufacturability & Yield DFM-DFY Flow





Pierluigi Daglio, Manager, Non Volatile Memory Design Flow, STMicroelectronics:
 "This analysis has been useful to demonstrate that the yield loss for the first topology was due to mismatch components, due to the need to generate constant differences and ratios of currents with transistor pairs. The yield has been increased reducing the relevant mismatch pairs after design centering with WiCkeD (Bandgap-Optimization Project from ISOQED2005)."

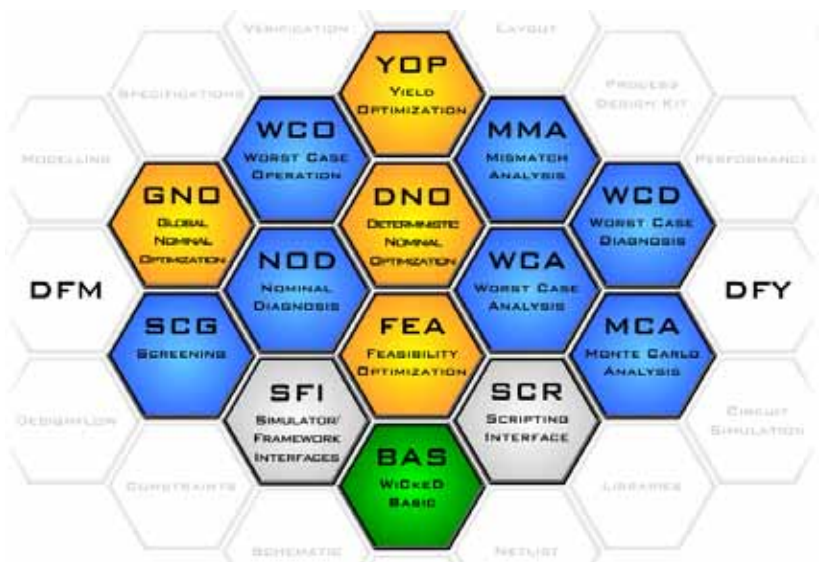

MunEDA's Design for Manufacturability and Yield (DFM/DFY) capabilities enable the circuit designer to

- Analyse and find the best circuit topology
- Fulfill given specifications and constraints
- Optimize nominal circuit performances
- Include process corners and statistical variations
- Maximize design robustness and yield

Design Analysis & Optimization Tools Overview

MunEDA offers numerous tools for circuits analysis & diagnosis and circuit optimization as well as interfaces to industrial standard and inhouse design environments and simulators

- Tools (required)** 
 - WiCkeD™ Basic - **BAS**
- Circuit Analysis Tools** 
 - Nominal Diagnosis - **NOD**
 - Parameter Screening - **SCG**
 - Worst Case Operation - **WCO**
 - Monte Carlo Analysis - **MCA**
 - Worst Case Analysis - **WCA**
 - Worst Case Diagnosis - **WCD**
 - Mismatch Analysis - **MMA**
- Circuit Optimization Tools** 
 - Feasibility Optimization - **FEA**
 - Determ. Nominal Optimization - **DNO**
 - Global Nominal Optimization - **GNO**
 - Yield Optimization - **YOP**
- Interface Tools** 
 - Scripting Interface - **SCR**
 - Simulator / Framework / Interfaces - **SFI**

Peter Gasteiner, Senior Vice President and General Manager of austriamicrosystems business unit Full Service Foundry:
 "Supporting MunEDA's state-of-the-art design analysis and optimization tool WiCkeD is a further step in the continuous improvement of austriamicrosystems DFM reference design flow. Supporting our customers to maximize their production yield and ensure robustness of their analog designs gives us a clear competitive advantage and strengthens our position as a leading supplier of specialty process technologies and extended foundry services."

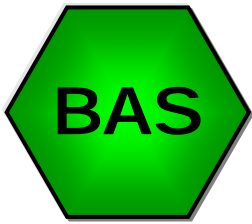
MunEDA Reference Application Cases

- 0,6 µm - Yield Optimization 110dB Op-Amp Automotive Applications
- 130 nm - Flash memory statistical analysis and optimization
- 90 nm - Bandgap design reuse and yield optimization
- 65 nm - DRAM I/O Sense Amplifier
- 180/130/90/65 nm Analog IP Porting

WiCkeD™ Basic

Tool Short Description

Feature Examples



BAS – WiCkeD™ Basic*

WiCkeD™ Basic delivers a powerful basic feature compilation to enable the circuit designer to do enhanced topology analysis, constraint setup and management as well as different analysis types for circuit performance, parameter sensitivity and correlation. Fully integrated in standard industrial simulators like Mentor® Eldo® / Eldo RF and Synopsys® HSPICE®.

- Constraint Editor
- Automated Parameter Setup
- Automatic Parameterization
- Topology Structure Recognition
- Parallel Simulation Interface
- Graphical User Interface
- Constraint Management
- Sensitivity Analysis
- Design Parameter
- Process Parameter
- Operating Parameter
- Parameter Sweeps
- Performance Setup
- Specification Entry



*BAS – WiCkeD™ is required for all further Circuit Analysis & Optimization Tools

Circuit Analysis Tools

NOD

NOD – Nominal Diagnosis

NOD enables the user to perform powerful analyses based on typical (nominal) process characteristics. The designer gets insight into dependencies between performances and parameters with very small simulation effort.

- Analysis of nominal design
- Manual optimization of nominal design
- Parameter influence analysis
- Parameter redundancy analysis
- Constraint limits
- Performance improvements, ...

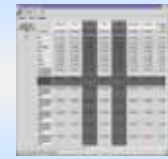


SCG

SCG – Parameter Screening

With SCG the circuit designer can filter during the design analysis and optimization process parameters with large and low influence on the performances and constraints. This can significantly reduce required simulation efforts.

- Automated Screening / Masking of design, process, and operation parameters
- Filtering based on sensitivities
- Interactive Filtering
- Automatic Filtering
- Simulation performance improvements, ...



WCO

WCO – Worst Case Operation

WCO is a powerful analysis tool that calculates and displays worst-case operating conditions. A special Worst-Case operation algorithm is minimizing/maximizing performances for lower/upper specification.

- Worst Case Operating Corners
- Calculation of worst-case performance values
- Non-linear performance characteristics
- Circuit Reliability Analysis
- Circuit Robustness Analysis, ...



MCA

MCA - Monte Carlo Analysis

MCA is one of the most powerful Monte Carlo Analysis tools on the market. Containing numerous tools and features for parametric yield analysis, contributors for yield loss can be detected and eliminated.

- Parametric Yield Analysis
- Mismatch Analysis
- Influence Analysis of Process Variations
- Contributor Analysis
- Performance distributions
- Scatter Plots, ...



WCA

WCA – Worst Case Analysis

With WCA the circuit designer is able to estimate the worst-case conditions for individual performance specifications. It determines partial and total yields for given specifications on circuit performances.

- Total yield estimation
- Partial yield estimation
- Consideration of operating conditions
- Consideration of process parameters
- Global process variations
- Local process variations (Mismatch)



WCD

WCD – Worst Case Diagnosis

WCD enables the designers to interactively improve and optimize the robustness for their designs. MunEDA's unique silicon proven Worst Case Distance methodology also enables the interactive optimization for yield.

- Specification driven design
- Parametric Yield Analysis
- Interactive Yield Improvement
- Contributor Diagnosis
- Worst Case Distance Algorithms
- Design Parameter Influence, ...

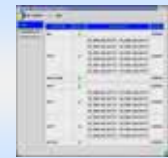


MMA

MMA – Deterministic Mismatch Analysis

MMA identifies and analyses mismatch-relevant transistor pairs on selected circuit performances. The variance of these local variations will be analyzed based on dependencies of device pair geometries.

- Mismatch pair detection
- Analysis of matching constraints
- Local process variations influence
- Information for yield optimization
- Fast deterministic algorithms
- Performances by mismatch effects



Circuit Optimization Tools

Tool Short Description

Feature Examples



FEA – Feasibility Optimization

FEA enables the circuit designer to automatically optimize the operating point of its design to fulfil all electrical/geometrical constraints. A feasible design represents a first step towards successful circuit optimization.

- Topology Analysis and Diagnosis
- Constraint fulfillment
- Algorithm Find Closest
- Algorithm Find Central
- Minimum change of constraints
- Maximum over fulfillment of constraints

FEA



DNO – Deterministic Nominal Optimization

DNO is a powerful optimization engine for automatic nominal circuit optimization. DNO improves circuit performance values by changing design parameters with unique gradient-based optimization algorithms.

- Least-Square Algorithm
- Parameter Distance Algorithm
- Automatic Performance Optimization
- Consideration of operating conditions
- Automatic Constraint Fulfillment
- Specification Driven Optimization

DNO



GNO – Global Nominal Optimization

GNO is a state-of-the-art stochastic optimization engine especially for optimization of circuits with non-linear behaviour. This enables to find global maxima and minima of the performance function.

- Performance specification bounds
- Parameters to modify
- Genetic Sizing Algorithms
- Adjustable number of iterations
- Time-Out
- Parallel simulation

GNO



YOP – Yield Optimization

YOP is one of the most powerful tools for automatic performance and yield optimization based on global and local process parameter variations. Active optimization of 6 sigma robustness levels and more are now possible.

- Automatic Yield Optimization
- 6+ sigma design optimization
- Consideration of operating conditions
- High efficient optimization engines
- Low simulation effort compared to Monte Carlo or Stochastic algorithms

YOP

Interface Tools



Simulator / Framework Interfaces

MunEDA supports the main industrial analog/mixed-signal standard simulators as well as customer in-house simulators.

Interfaces to

- SYNOPSIS HSpice / HSpiceRF Simulator®
- MENTOR GRAPHICS Eldo /EldoRF Circuit Simulator®

SFI



SCR – Scripting Interface

SCR is providing a powerful programmable interface to be used with the complete MunEDA tool set for integration of customer-specific algorithms and environments.

Supported languages and tools:

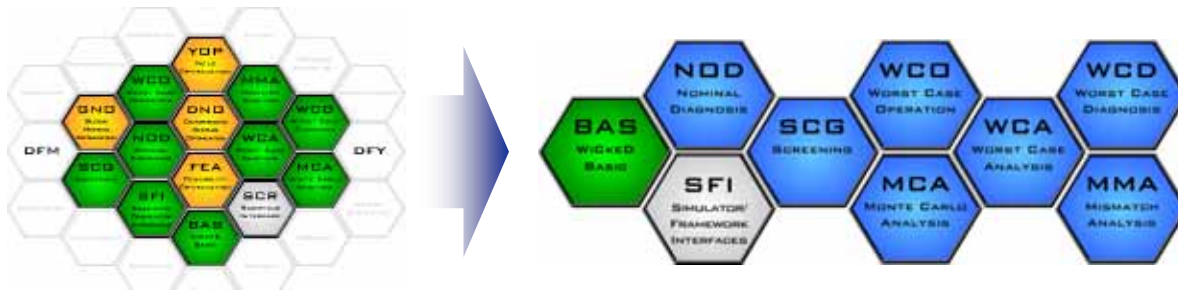
- Tcl/Tk
- Python
- Matlab
- R / S-Plus

SCR



Interactive Circuit Analysis & Optimization Flow

MunEDA Circuit Analysis and Interactive Optimization configuration contain the following MunEDA tools: WiCkeD Basic, Nominal Diagnosis, Screening, Worst Case Operation, Monte Carlo Analysis, Worst Case Analysis, Worst Case Diagnosis, Mismatch Analysis in combination with appropriate Simulator/Framework Interfaces.



Using the MunEDA analysis tools for circuit diagnosis and interactive optimization the designer gets a powerful toolset for intensive circuit design analysis. Using the MunEDA Circuit Analysis Tools existing problems or weaknesses in the design can be detected faster and solutions can be found quicker. All analysis features can be applied to the specific analysis and optimization problem and deliver large benefits especially for new circuit designs.

Fully Automated Circuit Optimization Flow

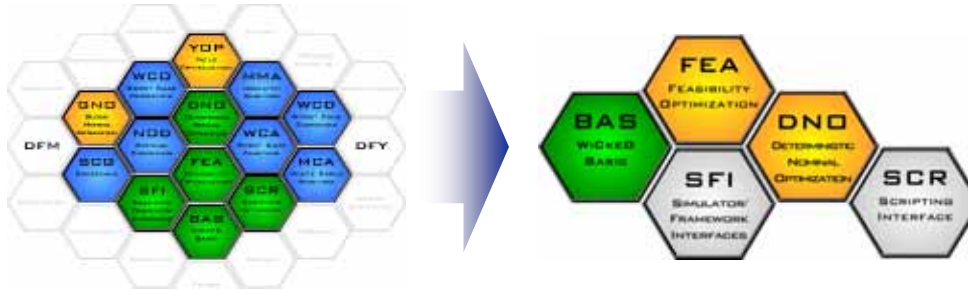
MunEDA Full Automated Circuit Optimization Flow contains the following MunEDA tools: WiCkeD Basic, Feasibility Optimization, Global Nominal Optimization, Deterministic Nominal Optimization, Yield Optimization in combination with appropriate Simulator/Framework Interfaces.



Using the full automatic optimization tools together with the BAS module the user can work with a fully automated circuit constraints, performances and yield optimization flow. This Full Automated Circuit Optimization Flow enables the user to work with MunEDA tools efficiently to save design time and improve product quality and assurance for state-of-the-art designs or standard technology migration projects.

Analog IP Porting

MunEDA Full Automated Circuit Optimization Flow contains the following MunEDA tools: WiCkeD Basic, Feasibility Optimization, Deterministic Nominal Optimization, Scripting Interface in combination with appropriate Simulator/Framework Interfaces.



Porting analog IP libraries to new technologies is a time-consuming task that traditionally has been performed manually. To speed up the main steps of specification-driven resizing, an industry-proven, fast and incremental circuit optimizer is required. IP porting of libraries particularly benefits from MunEDAs analog design analysis and optimization system that allow the user to apply an "optimization strategy" and also let it run automatically, because many circuit topologies are sized a few times each to target different specifications and technologies. For an Analog IP porting project...

Design Analysis & Optimization Flow Configuration Examples

DFM - Nominal Circuit Analysis & Optimization Flow

MunEDA DFM Nominal Circuit Analysis & Optimization Configuration contains the following MunEDA tools: WiCkeD Basic, Feasibility Optimization, Nominal Diagnosis, Screening, Worst Case Operation, Global Nominal Optimization, Deterministic Nominal Optimization in combination with appropriate Simulator/Framework Interfaces.



MunEDA DFM-Configuration Package delivers a complete solution for a Nominal Circuit Analysis and Optimization Flow. All features can be applied if there is statistical information from the manufacturing process available or standard nominal process information only. Main application field is the circuit constraint and performance analysis and optimization based on the nominal process data. DFM-Configuration Package is used to choose the best topology, verification of all constraints, and optimization ...

DFY - Statistical Circuit Analysis & Optimization Flow

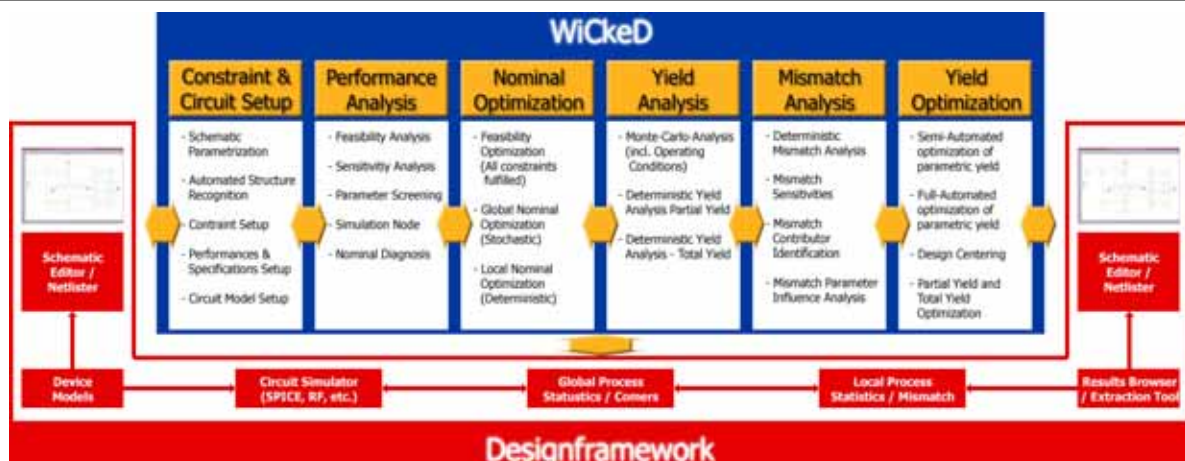
MunEDA DFY Statistical Circuit Analysis & Optimization Configuration contains the following MunEDA tools: WiCkeD Basic, Monte Carlo Analysis, Worst Case Analysis, Worst Case Diagnosis, Mismatch Analysis, Yield Optimization in combination with appropriate Simulator/Framework Interfaces.



MunEDA DFY-Configuration Package complements and enhances nominal-based DFM-Configuration with powerful tools for statistical circuit analysis and optimization. With DFY-Tools the designer is based on the given process data from the Fab able to optimize the parametric yield of the circuits already in the design phase. DFY-Configuration contains powerful tools for Yield Analysis and Optimization, Process Correlation Analysis, Yield estimation with enhanced Monte Carlo Methods ...

Besides these configuration proposals all MunEDA circuit analysis and optimization modules alternatively can be individually combined and applied by the user based on the specific circuit design task.

MunEDA Designflow Integration



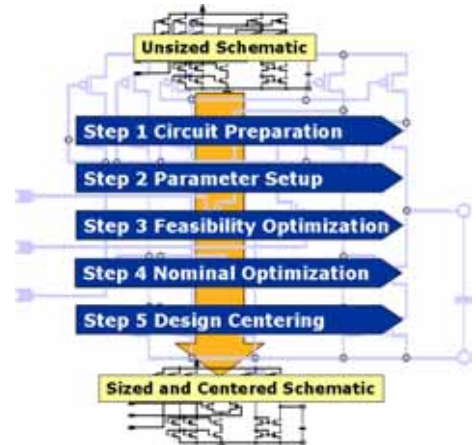
WiCkeD™ – 5 Step DFM/DFY Methodology

MunEDA offers a comprehensive and powerful software toolbox for interactive, semi- and fully-automatic analysis, sizing and design centering of analog and mixed-signal circuits. It is based on netlist and SPICE simulation using industrial standard and inhouse simulators.

WiCkeD™ enables the circuit designer to

- Analyse and find the best circuit topology
- Optimize nominal circuit performances to meet and fulfill given specifications and constraints
- Maximize design robustness and yield against process corners and statistical variations
- Design for Manufacturability and Yield (DFM/DFY)

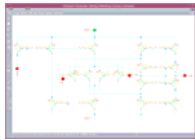
Following the standard DFM/DFY-Design Flow using WiCkeD™ is described in 5 main methodology steps (all values based on a real circuit example).



Step 1 – Circuit Preparation

Input

- Circuit Schematic
- Device Models



- Schematic Preparation – Device Parameters
- Testbench Setup
- Configuration of Simulation Environment
- Setup Model Libraries and Simulation Files
- Analyses Setup (DC, AC, Tran, XF, PSS, PNoise,...)
- Setup of Design Variables
- Setup of Output Expressions

Output

- Parameterized Schematic
- Model Preparation



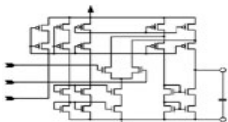
Based on the chosen circuit schematic the first step of the WiCkeD™ sizing and design centering flow is the preparation of the circuit and testbenches in order to be simulated, analysed and optimized. The characteristic of a circuit on transistor level depends on its topology, design parameters, process variation during production and operating conditions at the time of measurement. The designer is only able to change the design parameters, whereas the distribution of the process parameters and the specified range of the operating parameters are given. The designer's goal is to find design parameter values that make as many manufactured circuits as

possible fulfill their specifications in the full operating range. WiCkeD™ supports the designer with methods for analysing and optimizing her/his circuit design. For this reason it is necessary to parameterize the schematic to be able to change design parameter values in order to optimize the circuit to meet specifications and reach the best performance and yield. In Step 1 Circuit Preparation the schematic is parameterized. All device geometry parameters that are supposed to be optimized by WiCkeD™ are defined as design variables in the schematic cellview of the design framework environment using the initial values (if available) for optimization.

Step 2 – Parameter Setup

Input

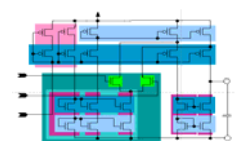
- Parameterized Schematic
- Specifications
- Parameters



- Automated Structure Recognition
- Automated Constraint Generation
- Constraint Management and Editing
- Parameter Setup (Design, Operation, Process)
- Circuit Performance and Specification Setup
- Mismatch Setup

Output

- Circuit Characteristics
- Constraints (Sizing Rules)



The number of sizing rules is usually too large to be set up manually for each device. WiCkeD™ contains an automatic structure recognition software that identifies basic circuit structures and assists the designer

by automatically creating sizing rules for these structures. Sizing rules are used in WiCkeD™ for diagnosis of the circuit, interactive sizing and automatic sizing.

WiCkeD™ – 5 Step DFM/DFY Methodology

Step 3 – Feasibility Optimization

Input

- Unfeasible Circuit
- Violated Constraints



- Automated Detection of violated constraints
- Analysis of best constraint optimization
- Automated Feasibility Optimization
- Design point best satisfies all constraints

Output

- Feasible Circuit
- Constraints fulfilled



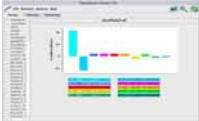
Of all possible sizings (=set of values of the design parameters), only a few satisfy all sizing rules. The restricted design space that contains all sizings that satisfy all sizing rules, is called the “feasible region”. For many circuits, the feasible region is very small (<1% of the total design space), and it is sometimes difficult to find a set of design parameter values that satisfies all sizing rules. WiCkeD™ Automated Feasible Optimization

automatically modifies design parameter values in order to find a feasible point in the design space. The user chooses between algorithms “find closest” and “find central”. “Find closest” modifies given design parameter values as little as necessary to fulfill the sizing rules. It is useful if a few rules are slightly violated, and the design is otherwise considered acceptable. “Find central” over-fulfills all sizing rules as far as possible. This is good for quickly finding an initial sizing.

Step 4 – Nominal Optimization

Input

- Feasible Circuit
- Operation Conditions



- Perform sensitivity analysis
- Trace of design parameters
- Circuit sizing using different optimization algorithms with worst case operating conditions
 - Deterministic (Local) Sizing
 - Stochastic (Global) Sizing

Output

- Nominal Optimized Circuit
- Optimized Performances



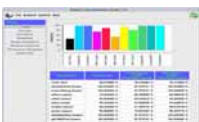
WiCkeD™ DFM Optimization provides three algorithms for automatic performance optimization. The designer enters performance specifications and selects parameters to be modified. Available algorithms are: 1) Least-squares: Performance specifications are fulfilled, but the optimizer does not try to over-fulfill them 2) Parameter distances: The optimizer tries to over-fulfill each specification as far as possible. Weight factors can be changed by the designer 3) Stochastic: Parameters are modified in a random manner over a sequence of generations with decreasing variance.

The first two optimizers are gradient-based. They converge quickly to the next local optimum of their goal function. Since the design space is restricted to the small feasible region, this is usually the only optimum. In rare cases with ill-defined, non-continuous performance functions over a large design space with few constraints, the later optimizer provide a global approach to optimization. For most practical circuits, gradient-based optimization outperforms global optimization regarding both algorithmic effort and quality of results.

Step 5 – Design Centering (Yield Optimization)

Input

- Nominal Design
- Process Statistics



- Monte Carlo Analysis
- Performance Distribution Analysis
- Parameter Distances Analysis
- Worst-Case Analysis and calculation of worst-case distances
- Inspection of worst-case operating parameters
- Optimization of worst-case points
- Automatic Yield Improvement

Output

- Centered Design
- Yield Optimized Design



After determination of yield with WiCkeD™ Monte-Carlo Analysis (able to handle full worst case operational parameter sets) the distribution of the performances as well as the parameter distances are measured and analysed. The next step is a worst case analysis and the calculation

of the worst parameter distances used for Design Centering and Yield Optimization. The user can choose between an iterative optimization method or an automated yield optimization engine to increase the parametric yield to the desired maximum. Design is ready for Layout!

Selection of MunEDA Customer Testimonials

Günter Kornmann, Director Analog Mixed Signal Designflows, Infineon Technologies AG

"WiCkeD is Infineons state of the art DFM-DFY tool in front-end design and fully integrated into Infineons Communication, Automotive and Memory Designflow. It is used since 2002 in more than 300 design and tape-out projects with Infineon in RF Design, High-Speed Analog, High-Speed Digital, Automotive Power, Embedded Memory, Enhanced Digital Cell Library Modeling, and other applications."

**Carlo Roma, CAD Engineer, STMicroelectronics**

"This analysis has been useful to demonstrate that the yield loss for the first topology was due to mismatch components, due to the need to generate constant differences and ratios of currents with transistor pairs. The yield has been increased reducing the relevant mismatch pairs after design centering with WiCkeD (Bandgap-Optimization Project from ISQED2005)."

**Thomas Hötzel, Chief Technology Officer, ZMD AG, Dresden**

"After testing MunEDAs design and yield optimization tool WiCkeD in some very successful pilot projects, we chose it for analysis and optimization of analog and mixed-signal circuits and towards increased yield and robustness of our golden IP library."

**Thomas Hsieh, R&D Associate Vice President, Faraday Technology Corporation**

"MunEDAs WiCkeD showed the capability as an optimization tool in the key role of our IP porting project. The capacity is a general issue for the simulation-based optimization tool. We successfully could demonstrate the circuit optimization process through the comprehensive GUI and script based flow."

**Thomas Ramsch, director of design support at X-FAB**

"Designing mixed-signal ICs is challenging and complex. We are pleased to add MunEDAs methodologies for circuit performance, statistical analysis and yield optimization to our full statistical modeling support. This powerful software helps our customers make their analog/mixed-signal designs more robust and get to market faster."

**Sancho Park, CEO of DAOU Xilicon, Korea**

"MunEDAs solutions address the most critical problems of todays circuit design - the decreasing manufacturing yield and thus robustness and reliability of designed and produced circuits. MunEDAs tools accurately predict and maximize the expected manufacturing yield and help the designers to identify critical structures within the circuit. The combination of MunEDAs DFM-DFY solutions and DAOU Xilicons expertise in the Korean market will help our customers to increase design efficiency as well as product yield and reliability."

**Robert Bosch GmbH (From ANASTASIA report)**

"Using the WiCkeD tools from MunEDA the designer undertakes a sequence of steps and methodologies that guide to a ready sized analog circuit. Within these steps both the operation region (temperature, supply voltage) as well as the statistical process variations will be considered. Additionally the developer gets estimation about the expected yield. With the consequent use of these methods at least 2 redesigns per year can be saved. This leads to improved time-to-market and lower development costs."

**Harald Schmidt-Habich, Principal Design Methodology, Automotive, Infineon Technologies AG**

"WiCkeD has been seamlessly integrated in Infineons Automotive Designflow for several flow versions. The carefree operation of WiCkeD is starting from the design framework and is used for semi-automatic circuit sizing. This tool and integration has shown to be very valuable for the designers because it allows them to use a completely GUI-based operation of WiCkeD inside the design framework. The database and ADE states are used to keep the information consistent and the designer's setup effort small."

**Dr. Gerhard Rappitsch, Principal Engineer DFM austriamicrosystems AG**

"A yield optimisation of an IP block was carried out using automated simulation based design centering and verification by experimental results. First, critical process parameters have been determined by sensitivity analysis allowing the improvement of production yield for the initial design by adjusting the PMOS threshold implant dose. In a second step a new set of design parameters was determined by simulation based yield optimisation where the goal was to keep the device area as small as possible and to maximize the worst-case-distance. The quality of the simulation results heavily relies on the accuracy of SPICE simulation models (Monte Carlo models) reflecting the global and local variations of the production process."

**Pierluigi Daglio, NVM AMS Flows & Methods Manager, STMicroelectronics:**

"WiCkeD is a perfect tool for circuit analysis, design optimization and yield enhancement. STMicroelectronics has used WiCkeD based on Mentor Eldo circuit simulation in numerous benchmarks and real applications and proved it helps to design more robust circuits with a better yield."





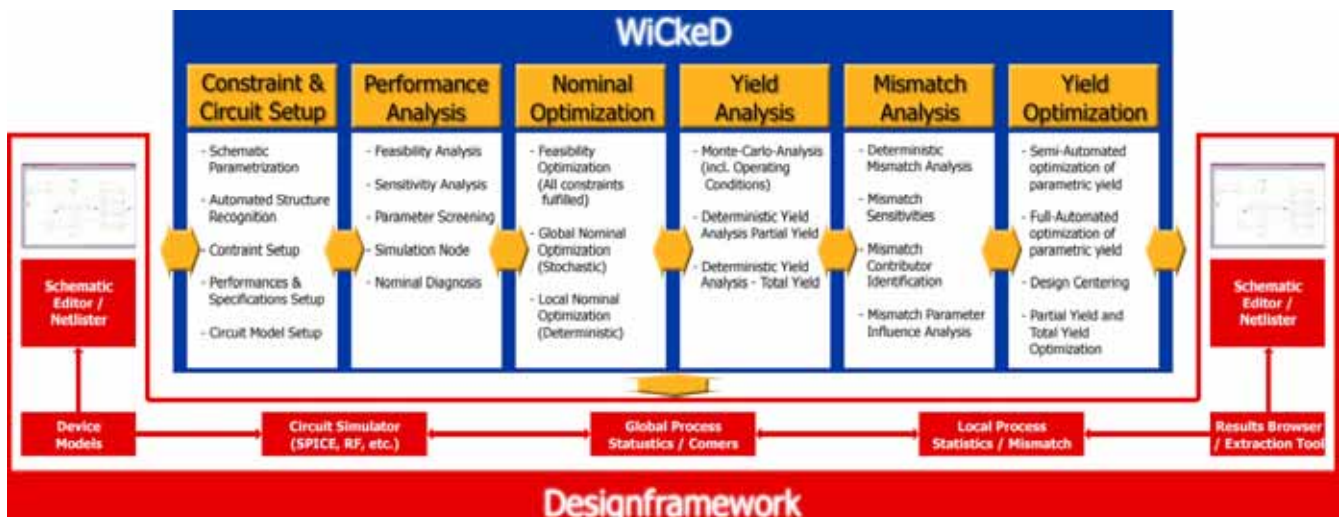
University Program

The MunEDA University & Research Program provides easy and cost effective access to MunEDA's software tools and solutions for universities and research organisations and institutes to be used for non-commercial teaching and research activities. This service is available to academic institutions and publicly funded research laboratories worldwide and requires a special check-up by MunEDA if you fulfil these conditions. Apart to other of such programs there is no membership fee required to participate in this program.

For further information please contact us directly.



MunEDA Designflow Integration



Application Case: Hierarchical Simulation and Optimization of a PLL

Circuit & Application

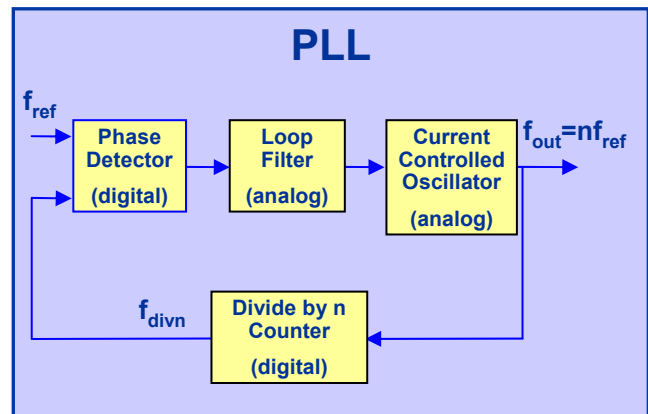
The circuit is a phase locked loop with the following Performance criteria: PLL lock time, attenuation factor and natural frequency. Process technology used was 130nm.

Problem Formulation and Goals

The hierarchical simulation was used, but serious compute resource problems arose as well as data inconsistency.

Design Problems without WiCkeD™:

- Required memory too large: 2900 MB
- Simulation time too high: 191 min
- Data consistency not guaranteed.



Solution using WiCkeD™

It was necessary to increase the resource efficiency. Using WiCkeD™, the problem was solved within three design steps:

Step 1 – Improvement of sequence control

By using WiCkeD's database the consistency of data was guaranteed. The hierarchical simulation was correctly controlled with the help of WiCkeD's script control. The memory requirement was halved.

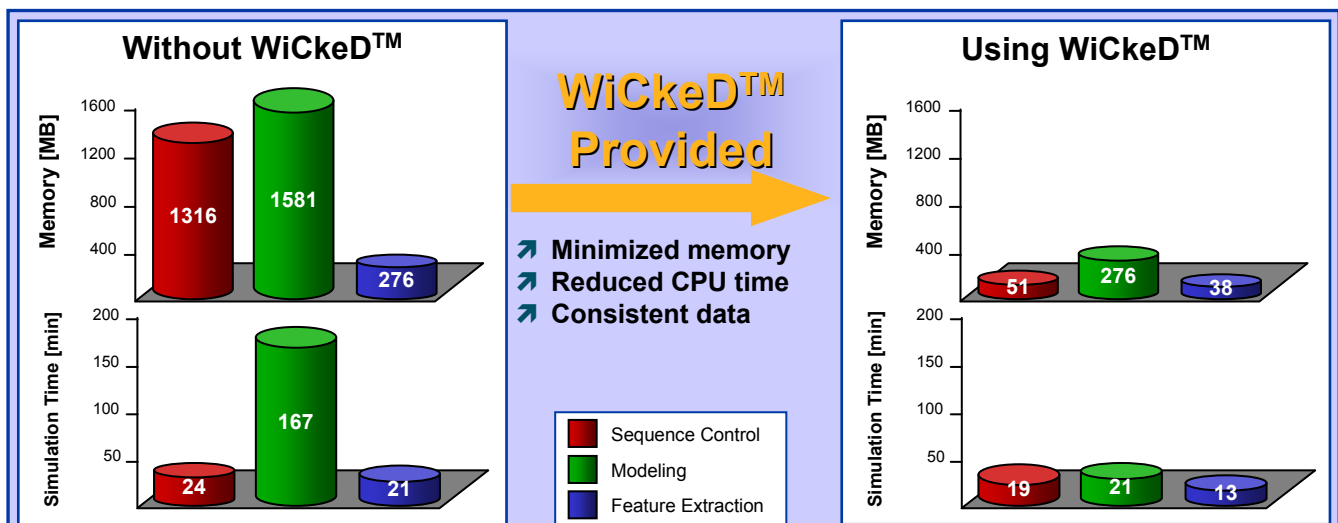
Step 2 – Improvement of Modeling

By shifting the borders from analog modeling to digital modeling within the single blocks, it was possible to reduce the simulation time. Also, the memory consumption was further decreased.

Step 3 – Improvement of feature extraction

The frequency of a rectangular signal was extracted by just reading the times of the rising slope. Therefore, the amount of data was reduced which reduced the memory consumption.

WiCkeD™ Results



Results - BMAS05, Fast Autom. Sizing of a Charge-Pump Phase-Locked Loop (Infineon Technologies) published: - DAC 2006, A CPPLL Hierarchical Optimization Methodology (Qimonda - TUM)

See also: - Customer Reference Cases: www.muneda.com/Customers_Customer-Cases
 - Publications: www.muneda.com/Applicatons_Publications



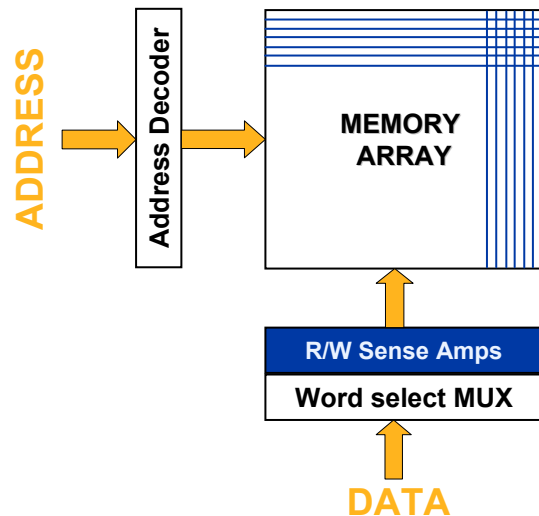
Application Case: Mismatch of Sense-Amplifiers in SRAM-Cells

Circuit & Application

Highly sensitive sense-amps used for charge detection in SRAM memories. Such memories require 6 sigma design for each cell. Process technologies used were 180nm, 130nm, 90nm, 65nm.

Problem Formulation and Goals

Predicting and improving the design quality in terms of performance, yield and robustness in the range of 6 to 7 sigma are a central concern in designing sense-amplifiers for use in SRAM cells. Many sense-amplifiers are on one die and therefore the yield of each has to be very high. All units of one chip have to work in order to make the whole chip work. A single failing sense-amp means the whole memory fails hence yield loss.



Solution using WiCkeD™

Step 1 - Feasibility Optimization

Using automated structure recognition, sizing rules were detected and met automatically in order to find a feasible solution as a starting point.

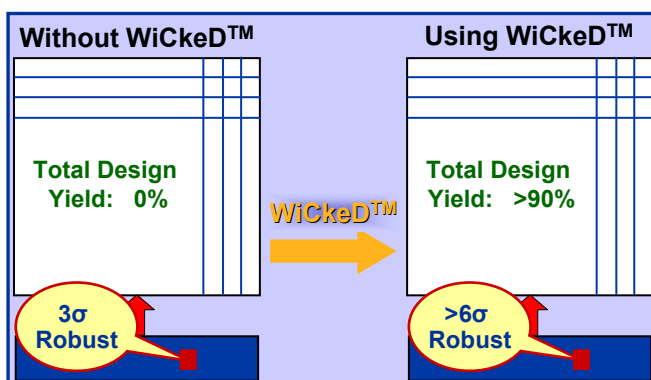
Step 2 - Nominal Optimization

Using WiCkeD's DFM Optimization all circuit performance specifications were fulfilled. As a result, yield analyses showed increased robustness and yield. However, statistical optimization was still necessary to get to the desired level of 6 sigma and a design yield of 99.9997%.

Step 3 - Yield Optimization

Using WiCkeD's Worst-Case Analysis the worst-case points were found. The worst-case point marks the region in the space of process parameters, where parametric faults are most likely to occur. Also, Mismatch Analysis showed the relevant mismatch pairs for the performances. Using WiCkeD's Yield Optimization functionality the worst-case performances were increased to a level of about 6 sigma and the existing mismatch effects were reduced to an acceptable minimum.

WiCkeD™ Results



- WiCkeD™ achieved 6 sigma robustness for each cell, starting from a conventional process corner optimized level of 3 sigma.
- After WiCkeD™ optimization the read-amplification sensitivity to the process variations was dramatically reduced.
- The SRAM-cells were sized to produce a total design yield of more than 90% as compared to a yield of close to 0% when using conventional process corner optimization.

Results published - MUGM 2006, 6T for embedded SRAM - 6σ design with WiCkeD™ (Infineon Technologies)
 - Advanced Radio Science 2006, Modelling of the parametric yield (Infineon Technologies)

See also... Customer Reference Cases: www.muneda.com/Customers_Customer-Cases
 Publications: www.muneda.com/Applications_Publications



Application Case: Sizing and Design Centering of Operational Amplifier

Circuit & Application

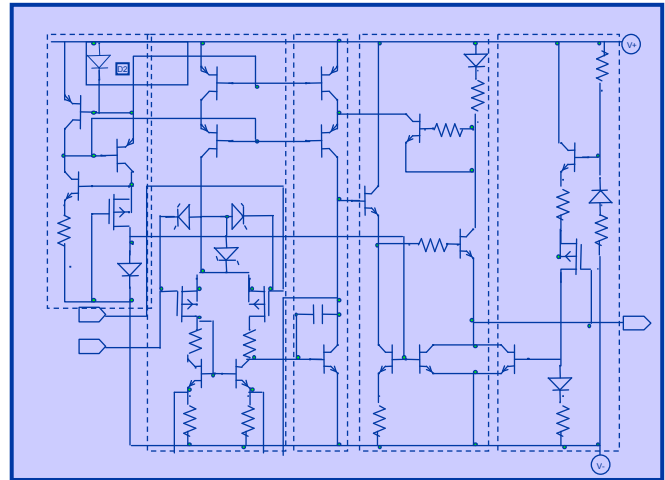
Operational Amplifier connected with biasing block generating all required bias voltages/currents. The circuit was designed for use in a Flash Memory. Process technology used was 500nm.

Problem Formulation and Goals

Particularly power consumption was too high and phase margin too low. In the required operating range the circuit did not work as specified, especially with respect to temperature and voltage. The yield of first silicon (done without WiCkeD™) was close to 0%.

Design Problems without WiCkeD™:

- Power consumption was too high.
- Phase Margin was too low.
- Design robustness was too low.
- First silicon yield was ~0%.



Solution using WiCkeD™

Step 1 - Adaptation of the component values

By adjusting the component values, internal constraints met their goals with respect to the saturation reserve and minimum area. Thus, functionality over the entire operating range was improved and robustness of the circuit increased.

Step 2 - Nominal Diagnosis

Utilizing WiCkeD's visualization of the dependencies between component values and quality, the developers modified the circuit interactively.

Step 3 - Automatic Nominal Sizing

Devices were sized with WiCkeD™ in a way that the circuit met the required specifications for the entire operating range.

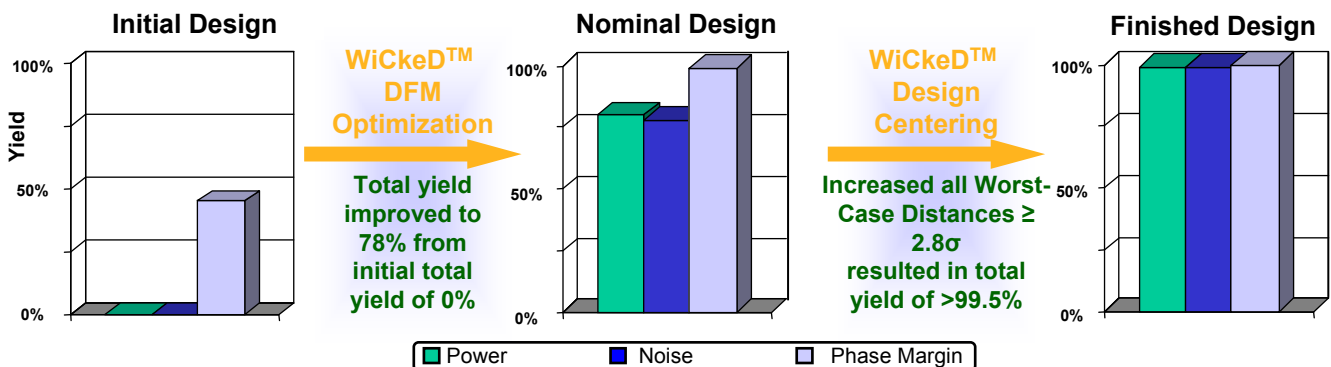
Step 4 - Tolerance Analysis and Worst-Case Diagnosis

Tolerance Analysis quantified the influence of process variations on the circuit. Using this information together with Worst-Case Diagnosis the designers were able to adapt the components to maximize robustness versus the process variations.

Step 5 - Monte Carlo Analysis

Monte Carlo analysis validated the expected parametric yield the designers achieved with interactive design centering.

WiCkeD™ Results



Results published - MUGM 2004, OPV and TIA Optimization (IMMS gGmbH, X-Fab)



See also... Customer Reference Cases: www.muneda.com/Customers Customer-Cases Publications: www.muneda.com/Applications Publications:



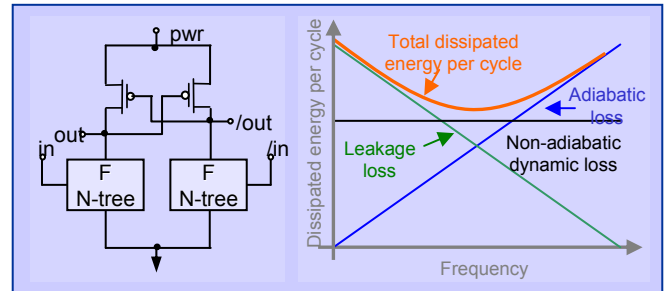
Application Case: Power and Yield Optimization of Adiabatic Logic-Gates

Circuit & Application

Adiabatic logic gates for very low power applications. Process technology used was 180nm

Problem Formulation and Goals

Energy dissipation was increasing dynamic power and leakage current because of the growing number of transistors on a chip. However, the capacity of batteries did not increase in the same way. Energy dissipation of the adiabatic circuits relied on analog properties of the transistors. The design goal was to reduce power and increase robustness and yield.



Design Problems without WiCkeD™:

- High power consumption
- Low robustness
- Low yield (40%)

Solution using WiCkeD™

Step 1 - Nominal Diagnosis

The impact of device W/L ratio on energy dissipation showed different trends for each source of dissipation. Using WiCkeD's DFM Diagnosis the performance dependency and parameter redundancies were identified and clearly visualized. The designers were able to analyze the link between component values and power dissipation to modify the circuit interactively with WiCkeD™.

Step 2- Nominal Optimization

Circuit devices were sized by WiCkeD™ such that the power dissipation was as low as possible without lowering the frequency. The input signals were shifted by -90° .

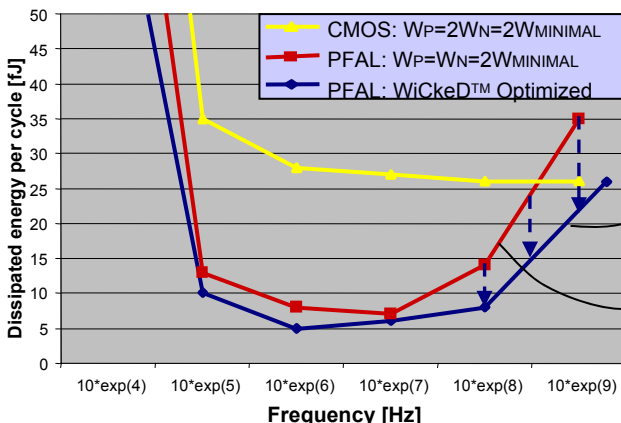
Step 3 - Tolerance Analysis and Worst-Case Diagnosis

The Tolerance Analysis measured the influences of the process variation of the circuit. Using this information together with the Worst-Case Diagnosis, designers were able to size the devices to maximize robustness with respect to the process variations.

Step 4 - Monte Carlo Analysis

Monte Carlo analysis validated the expected parametric yield the designers achieved with interactive design centering.

WiCkeD™ Results



Value added of using WiCkeD™:

- Power dissipation reduced 50%
- Crossover frequency over 1GHz
- Increased yield to ~97%

WiCkeD™
Analysis and
Optimization

Design before using WiCkeD™:

- High power consumption
- Low robustness
- Low yield (40%)

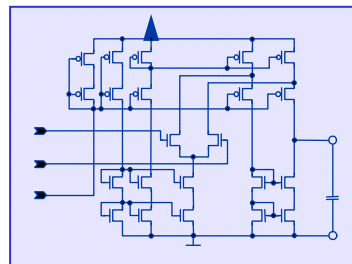
Results - LNCS (Lecture Notes in Computer Science, Reduction of the Energy Consumption in published Adiabatic Gates by Optimal Transistor Sizing, Springer Berlin (TUM))

See also... Customer Reference Cases: www.muneda.com/Customers Customer-Cases Publications: www.muneda.com/Applications Publications:



Circuit & Application

Folded Cascode Operational Amplifier with 22 transistors for which designer selected to allow 44 design parameters to be sized. There were 9 process variation parameters and 4 operating condition parameters. Process technologies used were 180nm, 130nm, 90nm and 65nm.



Problem Formulation and Goals

The original circuit had been produced in 0.18µm technology. The devices needed to be resized to be reused for each of the smaller geometry processes (130nm, 90nm and 65nm). The designer's goal was to quickly find a feasible solution with optimal yield.

Main tasks of process migration:

- Meeting sizing rule constraints
- Resizing for design reuse to meet specs
- Yield Optimization for all process variations

Solution using WiCkeD™

Based on specifications for each new process technology, the topology was analyzed with the initial sizing as start values. As expected, this resulted in 0% total yield and the circuit was not robust enough for the new process technology. WiCkeD™ used three steps to size the circuit for each new technology and achieved maximum yield each time.

Step 1 - Feasibility Optimization

Using WiCkeD's topology analysis and automated structure recognition, 190 sizing rules were automatically detected. WiCkeD's Feasibility Optimization aided the designer to match these rules and reach a feasible solution as starting point for the following performance and yield optimization steps.

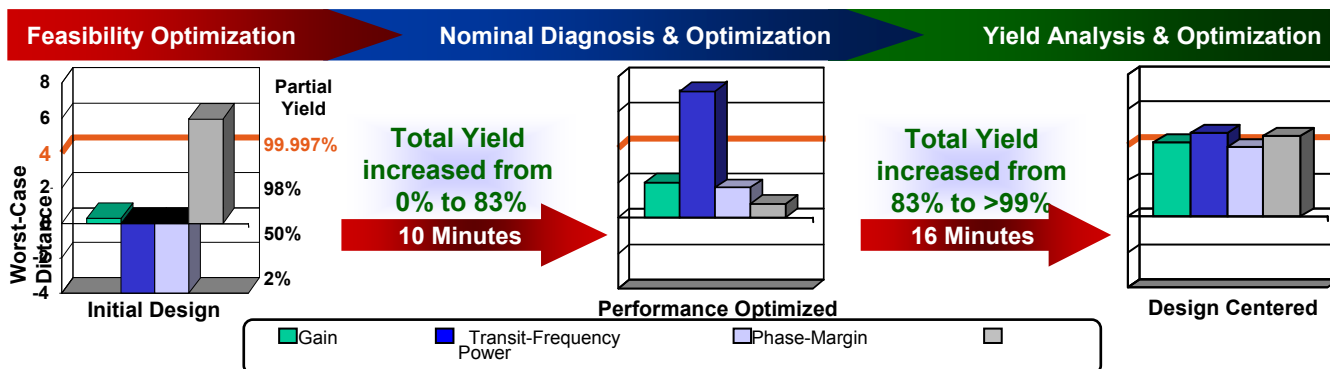
Step 2 - Nominal Optimization

WiCkeD's DFM Optimization brought all circuit performances to specification in 10 minutes of simulation using a deterministic optimization algorithm. Yield analysis of this performance optimized design showed an 83% increase in yield from the initial design.

Step 3 - Yield Optimization (Design Centering)

Using WiCkeD's Worst-Case Analysis, the designer was able to detect significant differences in robustness of the circuit performances. The partial yields of gain, power and phase margin were low. Using WiCkeD's Yield Optimization functionality, these performances were increased to a level of around 4 sigma. Because of topology specific trade offs, the high partial yielding transit-frequency was decreased to around 4 sigma. The overall total design yield of the circuit for the new process technology was increased to 99.99% (4 sigma). Simulation effort for this task was 16 min.

WiCkeD™ Results



Results - MEDEA+ Forum 2004, Yield Optim. of Analog Circuits with WiCkeD™ (Bosch - Infineon) published - EKOMPASS04, Systematic Analog/Mixed-Signal Desing...(Infineon Technologies - TUM)

See also: - Customer Ref. Cases: www.muneda.com/Customers_Customer-Cases
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Circuit & Application

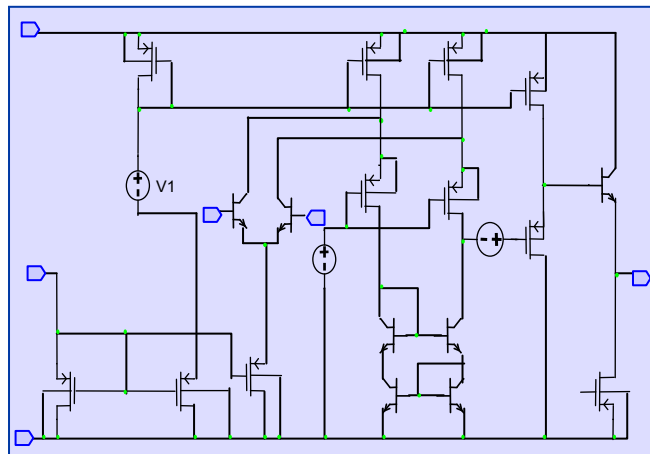
Folded Cascode trans-impedance amplifier used as IP in various other circuits with an open-loop testbench. Process technology used was 350nm.

Problem Formulation and Goals

The operating requirements for the circuit were to have a high bandwidth while maintaining a minimum of 60dB gain. Furthermore, the value for the second pole had to be high to increase stability.

Design Problems without WiCkeD™:

- Increase bandwidth substantially
- Keep the gain at or above 60dB
- Shift second pole further right



Solution using WiCkeD™

This design challenge included the frequent analog design problem of maximizing key performances while trying to minimize adverse impacts to other performances. The design flow using WiCkeD™ included 3 steps: circuit preparation utilizing automatic constraint analysis, achieving a feasible topology & optimizing performances.

Step 1 - Analysis: Circuit Preparation and Setup

WiCkeD's automatic constraint generation made it possible to quickly identify the current mirrors and level shifters. Additionally, the constraint analysis revealed that an auxiliary voltage source was needed. Furthermore, all design parameters (widths and lengths) for the devices the designer desired to be sized were identified as well as all performance parameters were defined at this step.

Step 2 - Feasibility Optimization

WiCkeD's Feasibility Optimization ensured all sizing rules were fulfilled. Additionally, the auxiliary voltage source was set in order to fulfill all constraints.

Step 3 - Nominal Optimization

By using WiCkeD's DFM Optimization, all circuit performances surpassed their specifications over the entire operating range. This improved the circuit characteristics and resulted in higher yield. Optimization time was minimized by using WiCkeD's parallel simulation capability distributing simulations onto various CPUs across the network.

WiCkeD™ Results

	Start	Previously Sized Manually	WiCkeD™ (1.5MHz)	WiCkeD™ (4 MHz)
Design Time		4 weeks	1 day	1 day
Bandwidth† (MHz)	0.38	1.5	1.5	4.0
2 nd Pole (MHz)	83	250	500	457

† Bandwidth optimized while maintaining a minimum gain of 60dB

Benefits of using WiCkeD™:

- Significant design time savings
 - ⊙ Design time reduced from 4 weeks to 1 day
- Noteworthy performance gains
 - ⊙ Bandwidth increased from 0.38 to 4.0 MHz
- Dramatic robustness improvement
 - ⊙ Second pole raised from 83 to 457 MHz

Results published - MUGM 2004, OPV and TIA Optimization (IMMS gGmbH)
 - EUROS01 05, Linear Regulators for High Temperature Applications (IMMS gGmbH)

See also... Customer Reference Cases: www.muneda.com/Customers_Customer-Cases
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MunEDA References by Industry



Automotive & Industrial



Consumer Electronic & Standard IC's



Memory



Sensors



Wirebound Communication



Wireless Communication

Interfaces / Platform Support:

- SUN-Solaris®, Linux
- Full Graphical User Interface
- Documented API (C++, Tcl/Tk, Phyton, etc.)
- Parallel Simulator Interface (LSF, SGE, rlogin, ssh)
- Export Interfaces (Matlab, R, SPlus)
- WiCkeD-Simulator and Framework-Interfaces:
 - Mentor Graphics-ELDO® ELDO-RF®, DesignArchitectIC®
 - Synopsys HSpice®, HSIM®
 - Inhouse Simulators (Qimonda-TITAN, etc.)
- Supporting industrial standard pdk (Process Design Kit)
- And customized to your environment!

MunEDA DFM/DFY Circuit Sizing Examples

Adiabatic Logic Gate
 Bandgap
 Buffer chain
 Bypass Filters
 Cascode Gain Stage
 CCO
 Charge Pump
 CML Converter
 Comparator
 Constant Voltage Source
 Current Mirror
 Current Source
 Current Mirror OpAmp
 Differential Amplifier
 Filter
 Folded-Cascode OpAmp
 Fully Differential OpAmp
 HF Circuit
 High Voltage Circuits
 Latch
 Level Shifter
 Low Voltage
 Operational Amplifier
 PLL
 Receiver
 RF-Circuits
 Ring Oscillator
 Sense Amplifier
 Sensor Circuit
 Single-Stage Amplifier
 Transistor
 Transceiver
 VCO
 Contact us for more examples & information

Selection of MunEDA Reference Customers



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