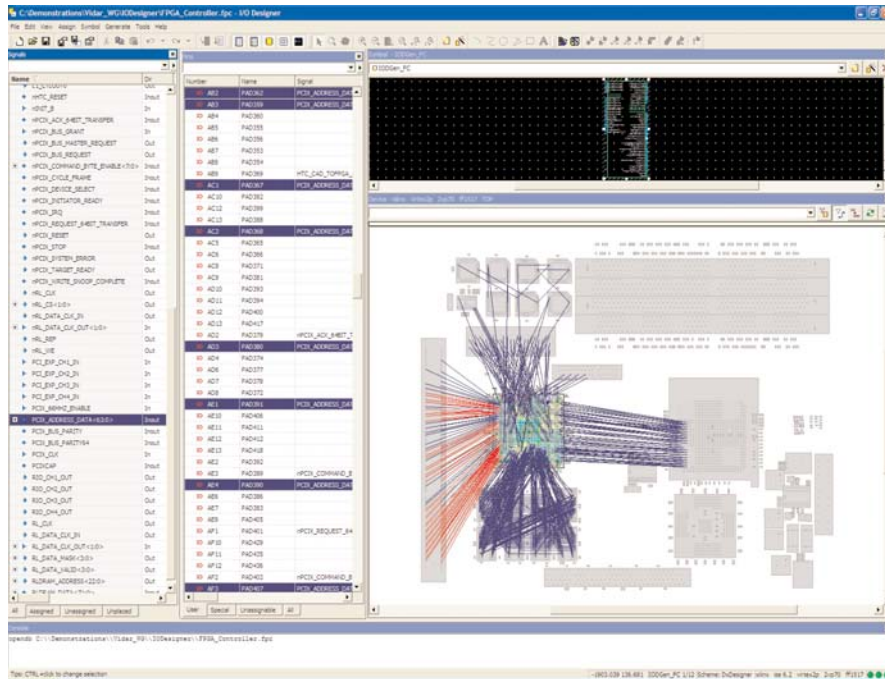


I/O Designer

The ideal focal point of advanced HDL, FPGA and PCB design

D A T A S H E E T



Major product benefits:

- Provides a graphical I/O design environment
- Serves as a bridge between your existing FPGA and PCB design flow
- Guarantees and maintains the consistency between the HDL, FPGA and PCB environments
- Supports migration to larger or smaller devices
- Automatically detects changes in HDL, FPGA and PCB related files
- Provides an automated flow, thus eliminating error prone manual tasks
- Assists with defining optimal I/O assignments for both the FPGA and the PCB

I/O Designer's graphical and spreadsheet based design environment.

Overview

The trend towards ever-larger FPGA's shows no sign of slowing, with some devices now offer over 1500 user-definable I/O pins. But taking advantage of all of those pins and getting the maximum system benefit afforded by FPGA's, with their unique ability to swap pins, can be a time-consuming, error-prone and costly task. These new devices require a tool that automates the process of connecting pins to the PCB and brings the FPGA and PCB design teams together in a common environment so that they can quickly see the ramifications of their decisions on the overall system.

To help with the growing demands of FPGA and PCB design, Mentor Graphics® offers I/O Designer™, a fast and efficient solution for assigning the I/O of your FPGA to device pins. By maintaining a library of FPGA's from several vendors, I/O Designer supplies all of the necessary information about each pin of the selected device. It also leverages FPGA vendor design rules and design rule checks (DRC) for pin definitions. By combining this knowledge with a high-level description of the FPGA, designers can assign the board-level signals to pins on the device. And this can all be done while viewing a footprint of the FPGA and its relation to the other board-level components using actual PCB placement data. Using a unique 'unraveling' algorithm, and by adhering to the vendor-defined rules for the FPGA, I/O Designer can quickly clean up what would otherwise be a tangled mess for the PCB designer. In addition, I/O Designer can create and/or update both FPGA symbols and schematics on which those symbols reside. Finally, to help take full advantage of the swappable nature of FPGA pins, I/O Designer creates the necessary swapping rules and makes those available to the PCB tools. This enables the PCB designer to swap pins but only within a sanctioned subset of legally defined alternates.

Data Management

I/O Designer oversees the consistency between the FPGA and PCB flows by acting as a data management tool, continuously assessing each flow and handling any changes that occur. Pin swaps carried out on the PCB are picked up by I/O Designer and the necessary files, including the FPGA P&R and synthesis files, can be updated using a design synchronization 'wizard' closing the loop between I/O Designer and the PCB and FPGA tools.

I/O Designer offers a unique process for moving through the design flow, from the top-level HDL description to the schematic-level symbol, as well as to the physical pin information necessary for the FPGA place and route tools. It monitors changes made in FPGA place and route tools, as well as those made in the Mentor Graphics PCB schematic and layout tools, and notifies the user of any out-of-sync data. In addition, I/O Designer offers a central solution for the digital design engineer performing the HDL design and the physical implementation of the FPGA, as well as for the board designer using the device symbol.

Design Cycle Time Reduction

To decrease design cycle time, I/O Designer allows designers to work in parallel with PCB and FPGA designs. This parallel process requires an initial layout of the board, as well as a symbol of the device. Three interacting design areas influence the final pin assignment of a device, including:

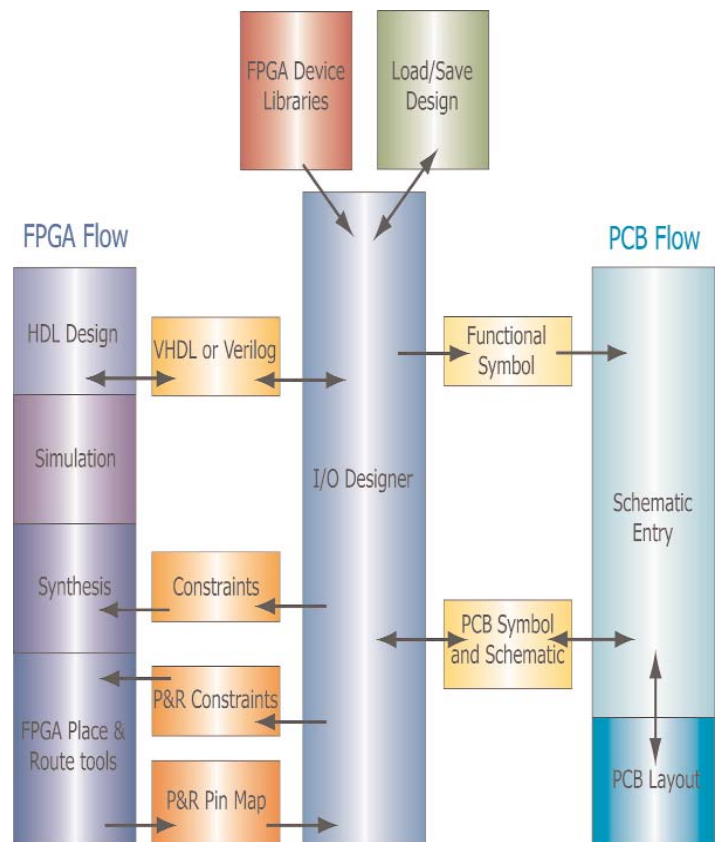
- Functional specification changes in the HDL description
- FPGA Place and Route related changes in the pin assignment
- Back annotation of PCB layout changes (e.g. pin swaps to facilitate better PCB Routing)

Using just a top-level description of the FPGA, schematics and symbols can easily be created, enabling the rest of the team to quickly begin working on their portion of the design.

Symbols and Schematics

I/O Designer supports most industry symbol standards by offering a customizable library of pin and symbol shapes. It also offers advanced features for importing and exporting symbols and schematics, including the ability to export Mentor Graphics native symbols and schematics for Design Architect®, Board Architect™, DxDesigner™, Design Capture™, and DesignView™, as well as the ability to import schematic symbols via EDIF and XML. I/O Designer also provides an easy to use interface that contains a schematic symbol window that allows signals or pins to be 'dragged and dropped' and a graphical display of footprints to map signals to pins. This interface allows for on-the-fly updates that are immediately

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I/O Designer integrates the FPGA and PCB design flows.

reflected within the PCB tools and written out to the FPGA tools.

Hardware Platforms

- PC
- Sun SPARCstation

Operating Systems

- Windows 2000, XP
- Solaris 2.6 or later
- RedHat Linux 7.0 or later

System Requirements

- 1 Gig free disk space
- 512 MB system RAM recommended

License Configuration

- Time based
- Floating: Windows 2000, XP, Solaris, Linux
- FlexLM protected

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