

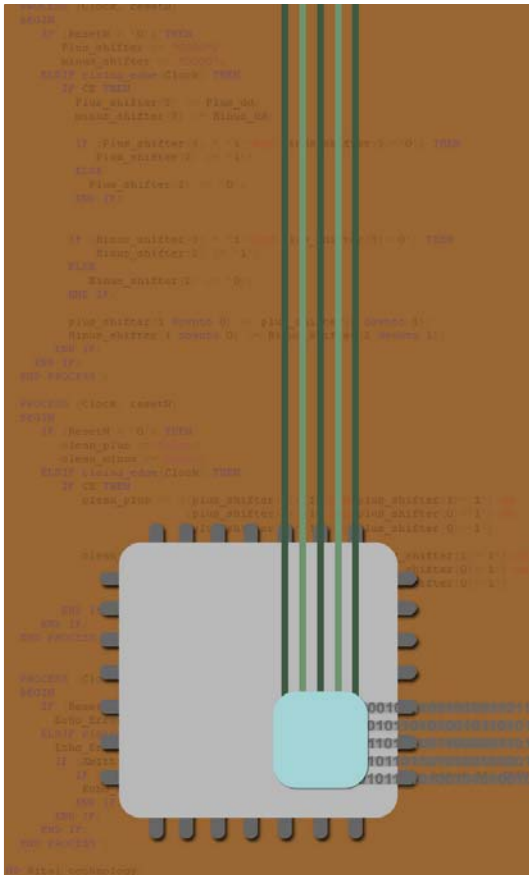
# MIL-STD-1553 IP Core for FPGAs



# RT1553FE

For 1553 Remote Terminal  
Simple Implementations

Robust, Reliable, Stable  
MIL-STD-IP-Cores

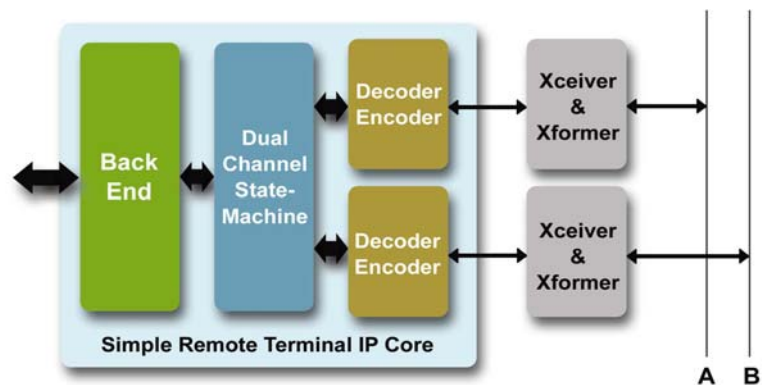


## More IP Cores from Sital:

- MIL-STD-1553 Remote Terminal DDC\* enhanced mini-ACE\* interface
- MIL-STD-1553 Bus Monitor
- MIL-STD-1553 Bus Controller

## Key Features and Benefits

- Offers the best gate count in the industry
- Supports any even clock frequency
- Does not require CPU for management, no SW required
- Suitable for any simple MIL-STD-1553 RT implementation
- Modular architecture allowing flexible implementations
- Provided with full verification environment
- Passed full validation testing by 3rd party
- Reduces risks related to parts obsolescence
- Uses vendor and technology independent IEEE-1076 VHDL design and coding



Sital's MIL-STD-1553 IP products, based on an innovative vendor-independent architecture, offer uniquely portable and flexible solutions for any PLD/FPGA device. They were developed following the company's unflinching commitment to quality and excellence along with strict adherence to meeting the stringent requirements of the military specifications. Designed from the ground up for use in the aerospace and military industries, Sital's products have been praised by customers who have recognized their benefits and reliability over traditional products.

## Specifications

### Compatibility

- MIL-STD-1553B Notice 2
- RT Validated according to test plan from MIL-HDBK-1553A
- 1Mbps Data Rate

### FPGA Requirements

- 32 RAM elements of 16 bits each
- Typically less than 5% of device
- 10 pins to connect to transceiver
- Standard FPGA pads

### Clock

- Any even frequency over 12MHz

### FPGA Net-lists provided

- **Xilinx:** All FPGA Families, including: Virtex II, Virtex II Pro, Virtex-4, Spartan-2, Spartan-2E, Spartan-3, Spartan-3E
- **Altera:** All CPLD Families, including: Stratix, Stratix II, Cyclon, Cyclon II
- **Actel:** All Families, including Space Grade FPGAs.
- **Atmel:** All Families
- **QuickLogic:** Selected Families

### RT1553FE Deliverables

- EDIF net list for desired FPGA family and clock frequency.
- User's manual.
- Sample VHDL code that incorporates the core.
- Synthesis script for sample code.

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## A core for simple implementations

This MIL-STD-1553 IP Core is intended for small and simple Muxbus implementations., where relatively short messages are sent over the bus. Such messages are typically composed of a command pointing to a Sub Address (SA), indicating the number of words for that SA.

For example – on/off messages, a periodic update messages, etc.

## Smallest Gate Count

Sital's MIL-STD-1553 IP Core is the smallest in the industry. The following table shows the area usage in different FPGA devices:

Vendor	Product Family	Area Usage
Altera	Cyclone	823 LEs
Altera	Stratix	820 LEs
Xilinx	Spartan-2E	490 Slices
Xilinx	Virtex II	487 Slices

## Backend Interface

The RT1553FE interfaces with the back-end through simple address-data read and write "bus cycles".

- No CPU is required
- Simple integration with user's logic

## Manchester Decoder

The unique Manchester decoder can work with any even clock frequency from 12Mhz and up (for example, it could work with a PCI interface's 66 Mhz clock). Special algorithms for filtering out noise and disturbances in data are incorporated in the decoder.

## Advanced Verification

To ensure a reliable and robust product the core was developed using an advanced verification environment that includes a Random-Generation engine, Code-Coverage and assertion tools. All MIL-STD-1553B functions, requirements and performance were verified.

## 3rd Party Validation

The IP Core successfully passed the full MIL-STD-1553B Notice 2 RT Validation test, according to test plan from MIL-HDBK-1553A. The test was performed by an independent 3<sup>rd</sup> party.

## Simple Integration

A VHDL design sample that uses the core is provided, including:

- A Transceiver VHDL model that connects the core with 2 buses.
- A bus tester VHDL model that generates 1553 messages and checks the return replies.
- A top Test bench that instantiates all of these components to a working example.
- A synthesis script for the RT sample.
- A simulation script for compiling and running the core.

## About Sital Technology

Founded in 1993, Sital Technology is a leading provider of EDA (Electronic Design Automation) products and services. We combine representation of leading vendors such as Mentor Graphics, Opnet and ClioSoft, with training capabilities for design languages (VHDL, Verilog, PSL, SystemVerilog). Sital is also a high-level R&D center for Military communications, Network design, DSP and Image Processing.

SITAL Technology's key quality resource is its creative, talented and professional staff. Our engineers are veterans of the Israeli Air Force, who served in the technical units of the F-16 avionics systems. They gained knowledge and experience with the MIL-STD-1553 standard from the bottom up, both as design engineers for MIL-STD-1553 components and as technicians working on the aircrafts.

Among our many customers you can find NASA, Israeli Aircraft Industries (IAI), Rafael, Elbit, Astronautics, Tadiran, The Israeli Ministry of Defense, Elta, ITL Optronics, BAE Systems, RADA and many others.