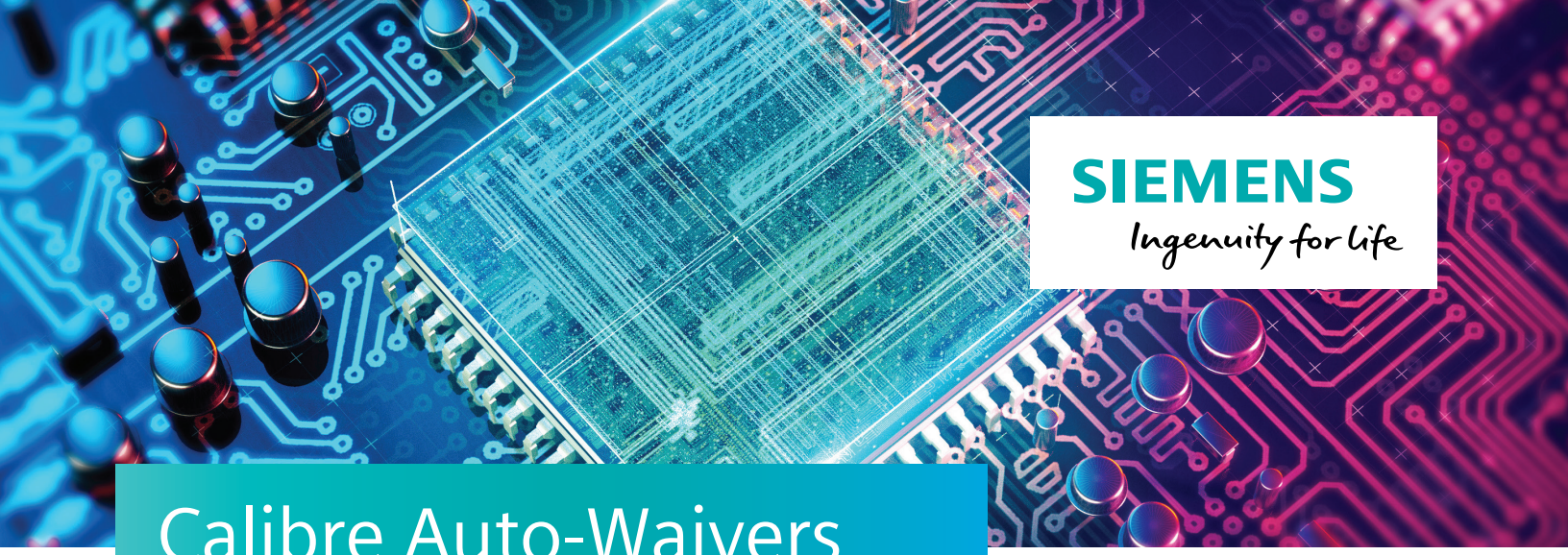


SIEMENS
Ingenuity for life

Calibre Auto-Waivers

Automated waiver management

Benefits

- Accurately identifies waived design rule violations in IP blocks regardless of hierarchical interactions
- Implements waiver management automatically during the Calibre nmDRC run without modifying golden rule file
- Uses a single layer for waiver identification, regardless of the number of checks with waived violations
- Reports all real errors, waived results and unused waiver markers for bookkeeping
- Uses pattern matching to provide acceptable margin of difference between a waiver marker and a top-level result
- Eliminates redundant error debugging
- Eliminates need to re-negotiate design rule violations in IP
- Ensures accuracy and consistency in waiver processing
- Provides standardized recording and tracking of waiver information for historical analysis across designs and processes
- Leverages existing Calibre DRC rule files and Calibre RVE™ ASCII results

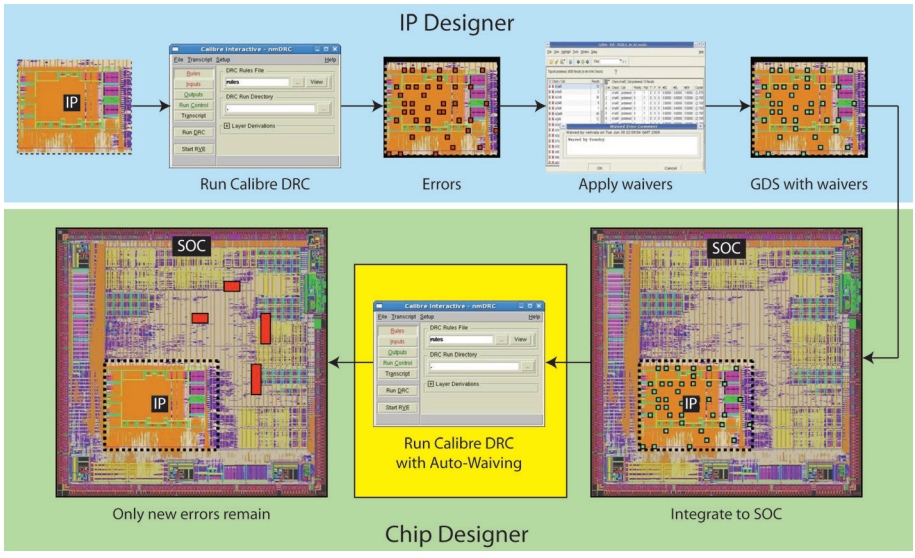
Introduction

Design rule waivers negotiated between intellectual property (IP) designers and foundries are rarely transferred to IP customers in a consistent manner, or in a format that allows for easy identification of the waived errors during DRC of the integrated design. Consequently, waived IP errors often reappear at the full chip level, indistinguishable from other DRC violations. This means the chip designer spends the same amount of time and energy debugging waived errors as true errors. Because integration designers don't own or create the IP, they have no option other than to contact the IP provider to identify and/or re-validate the waiver. These productivity "sinkholes" increase verification time without adding value.

Automated waiver management with Calibre

The Calibre® Auto-Waivers™ tool provides automated recognition and removal of waived design rule violations in external IP, eliminating redundant error debugging while ensuring that all waived errors are properly identified during full-chip verification.

The Calibre Auto-Waivers process uses industry-standard GDSII or OASIS layout



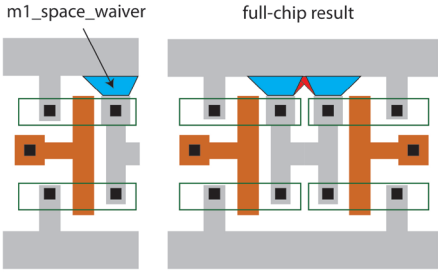
Calibre automated waiver management ensures IP quality while eliminating redundant error debugging and waiver negotiations during IP integration.

Calibre Auto-Waivers

formats to describe waived errors. As the IP designer validates the IP layout, error results approved by the foundry as waivable are incorporated back into the original IP cell as geometric data. Through the Calibre Auto-Waivers process, these waivers are created as separate cells for each rule check that contains a waived violation for an IP block, and instantiated back into the original IP block. Waivers for different rules are differentiated using a cell naming convention that associates the newly instantiated sub-cell to the rule generating the waived results. The cell name approach lets the IP designer place all waived results on a single reserved layer in the layout database, regardless of the number of checks in the rule file, keeping layout size and complexity to a minimum. For each process, the reserved layer can be specified by the foundry/fab, ensuring continuity and consistency across IP designs and IP providers.

The integration designer incorporates this merged IP layout geometry, including the waiver information, into an SoC design and runs the Calibre DRC process against the full chip. The Calibre nmDRC™ tool uses the waiver information to automatically modify its handling of rules to be waived during the DRC run for the specific checks and locations associated with the waiver geometry. This rules modification can be trusted because the waiver process and corresponding rule modifications are fully qualified as part of Calibre nmDRC's qualification by the foundry for the process and rule file. Through this approach, the waivers are now purely geometric, allowing the Calibre Auto-Waivers process to automatically and accurately remove them from the DRC output, regardless of how or where the errors appear hierarchically.

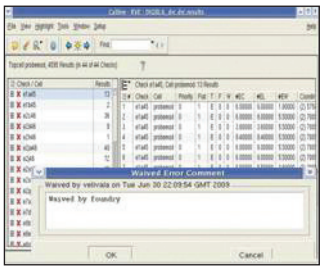
Because waived IP results may become modified in shape due to their contextual placement in the full-chip design, it is possible to obtain DRC results that do not exactly match the original waiver geometry. To provide an acceptable margin of tolerance against false errors, the Calibre nmDRC process performs the waiving process using pattern-matching criteria specified by the foundry for each waived rule.



Waivers that become modified in context are identified through pattern matching criteria defined by the foundry.

Using the continuous function ability of the Calibre eqDRC™ process, the Calibre Auto-Waivers tool compiles a list of waived results per cell and location, with properties indicating the exact margin of error determined during pattern matching. Once the design is DRC-clean, the chip designer can view all waived results to ensure that each is safely within the acceptable error margin. Any waived error uncomfortably close to the specified margin can be analyzed to determine if a design adjustment is needed to avoid a manufacturing issue. Alternatively, these waivers may indicate locations that warrant a higher level of testing post-manufacture. Once the designer is confident that none of the "marginal" waived errors pose a potential problem, the design can proceed to tapeout. Performing the waiver review after the DRC-clean run avoids the need to perform this step after each DRC iteration, but still ensures that any marginal waived errors are examined before tapeout. This final review assures the designer that any waived error with the potential to impact the design's manufacturability, even marginally, has been evaluated.

In addition to waived results, the Calibre Auto-Waivers tool also reports waived locations not encountered during DRC. Design features sometimes create an error in isolation that is eliminated when the features are placed in context. Alternatively, a waiver geometry may not meet the level of marginality required to eliminate a final error result. Reviewing these unused waiver geometries helps track the types of results that are typically corrected in context. Together, the list of waived results and list of "unused" waivers provide the integration designer with the documentation needed to record the history of waiver management in the design.



Calibre Auto-Waivers shows DRC violations grouped by "real" errors, unused waivers and waived errors.

Since time to market is a key factor in the success and profitability of an IC, any process that reduces verification time while also improving the quality of results is highly advantageous. The Calibre Auto-Waivers tool not only shortens the verification process, but also ensures accurate processing of all waiver information on every DRC run. Because it uses existing industry standard formats and tools, the Calibre Auto-Waivers process can be adopted without requiring significant change in current design flows.

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