Calibre PERC

Advanced reliability verification

electrical errors that can result in reduced yield, defect escapes to customers, and delayed failures in the field.

Advanced reliability verification ensures the robustness of a design both at schematic and layout levels by checking against various electrical and physical design rules that define IC performance standards and reduce susceptibility to premature or catastrophic electrical failures.

Calibre® PERC™ is specifically designed to perform a wide range of complex reliability verification tasks using both standard rules from the foundry and custom rules created by a design team. Users can insert reliability verification into their existing design flows with Calibre PERC as part of an integrated Calibre platform for cell, block, and full-chip verification. Combining rules expressed in SVRF and the Tcl-based TVF language across all applications provides users with flexibility to meet

Benefits

- **Improve design reliability** – Eliminate potential electrical violations that can reduce product life or cause catastrophic electrical failure

- **Improve design accuracy** – Same trusted device recognition as Calibre nmLVS; part of award-winning Calibre product line

- **Zero risk** – Fully compatible with the Calibre platform, Calibre PERC integrates easily into existing signoff flows

- **Reduce time to market** – Timely execution ensures production schedules are maintained

Features

- Advanced reliability verification – Processes the most complex circuit reliability requirements of today's leading-edge technologies

- **Automated checking** – Insert reliability checks into existing design flows for cell, block, and full-chip verification

Calibre PERC – The next evolution of circuit reliability verification
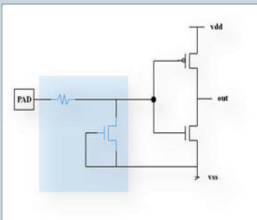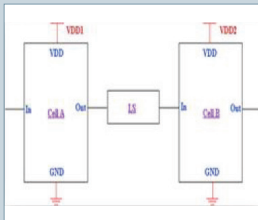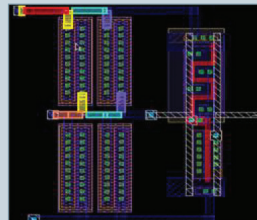
Reliability is a growing concern for integrated circuit (IC) designers, especially in products such as communications, medical, and transportation, where reliability and performance are not just market differentiators, but critical components of safe and effective operation. Many reliability checks are difficult to check using traditional DRC, LVS and ERC tools, and can potentially affect a wide range of IC designs. Electrostatic discharge (ESD), electrical overstress (EOS), and latch-up are just some of these complex geometrical and

Custom	Digital	Post-layout
• Electrostatic discharge (ESD) checking • Electrical overstress (EOS) checking	• Cross-power domain checking • Low power verification	• Point-to-point resistance • Current density • Voltage-dependent DRC

Calibre PERC enables a wide range of complex electrical and geometrical verification requirements to ensure product reliability and performance.

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Features *continued*

- **Fully compatible** – Rule decks available from major foundries

- **Fully customizable** – Programmable SVRF and the Tcl-based TVF platform provide a highly flexible, user-configurable tool for fast and accurate development of customized rules

- **Netlist-based** – Analyzes source or layout SPICE netlists

- **Fast runtime** – Proprietary automated hierarchical and logic injection technologies provide a scalable solution with fast runtimes

the specific and evolving needs of their design teams, while ensuring compatibility with all foundries.

Contrary to traditional electrical checks using a single device/pin to net relation, reliability requirements can often only be described by a topological view that combines both circuit description and physical devices. Calibre PERC's ability to use both netlist and layout (GDS) information simultaneously to perform electrical checks that incorporate both layout-related parameters and circuitry-dependent checks enables designers to address these complex verification requirements. In addition, Calibre PERC can employ topological constraints to verify that the correct structures are in place wherever circuit design rules require them.

Calibre PERC can automatically identify complex circuit topology on a design netlist, either streamed from the schematic or extracted from the layout. It examines the specific constraints defined by the design team, whether they are electrical or geometrical. Calibre PERC rule decks may be easily augmented to provide verification beyond standard foundry rule decks to include custom verification requirements.

Advanced reliability verification

Electrical overstress

In place of time-consuming simulation, Calibre PERC uses static voltage checking to automatically propagate voltages throughout the whole design. Users define some or all input voltages, and rules for propagating these voltages across different device types. Calibre

PERC then performs the static analysis and assigns the correct voltages to all the design internal nodes.

Electrostatic discharge

ESD checks typically include several considerations, such as identifying possible areas of electrical failure, the geometrical constraints of device dimensions, the number of device fingers, distance from supply pads, and the different circuitry combination on multiple power domains.

Calibre PERC can not only identify the circuit elements that make up your ESD protection structures, it can also ensure that they have the correct values, that elements are properly connected with respect to the core IC, and that no elements are missing.

Multiple power domains

Low-power and multiple-power verification requires system knowledge and careful tracking of signals crossing power domains. Calibre PERC can identify signal lines crossing directly from one domain to another in designs that require different voltages for multiple domains. It can also verify additional ERC configurations between multiple power domains, making it equally easy to verify the layout or the schematic for early detection, and avoid silicon failure.

Post-layout verification

Transistor placement and design interactions can have a significant impact on design robustness. Such interactions include:

- Point-to-Point resistance (P2P)
- Current Density (CD)
- Voltage-Dependent DRC
- Hot gate/diffusion identification
- Layer extension/coverage
- Device matching

Post-layout verification can incorporate complex geometrical parameters into Calibre PERC checks, combining both electrical and geometrical data in a single verification step. In addition, rather than running verification on an entire design, Calibre PERC's topological capabilities enable users to quickly and accurately check specific sections of designs for these types of issues.

Integrated debugging environment
Calibre PERC output can be customized for your design flow, while Calibre RVE provides a results viewing and debug environment that can highlight results and geometries, and access connectivity information.

Comprehensive reliability solution
Accurate and repeatable reliability verification is now a critical capability. Calibre PERC is the only comprehensive solution capable of verifying geometrical, electrical, or combined constraints. As part of the Calibre platform, it also integrates easily into your existing signoff flows, with comprehensive debug provided by Calibre RVE. Calibre PERC provides an easy-to-use, automated and programmable verification solution for circuits on both the schematic and layout side, ultimately reducing cost and time to market, while providing the diagnostic insight to help you improve yield and device reliability.

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