SIEMENS
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# Calibre RVE

## Results Viewing Environment

The Calibre RVE interface is integrated into all popular layout environments, including the Pyxis® design environment, the Tanner design tool suite, the Calibre DESIGNrev™ chip finishing platform, Synopsys® IC Compiler, Synopsys IC Compiler II, Cadence® SOC Encounter®, Cadence Innovus®, Cadence Virtuoso®, Synopsys Laker™, Seiko, and Keysight. Whatever design environment you use, the Calibre RVE interface provides the debugging technology you need for fast, accurate error resolution.

### Features and benefits

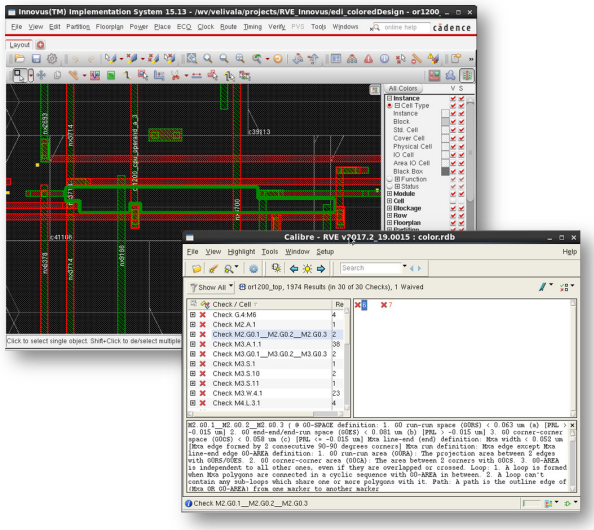
- **Universal integration with layout environments:** Using the Calibre RVE interface minimizes training and support overhead, and provides a single, consistent interface across all your design tools.
- **Fast debugging time for cell, block and full-chip designs:** Whether you have 10 or 106 errors, the Calibre RVE interface provides fast response time with minimal memory overhead
- **Single platform for all Calibre results:** The Calibre RVE interface provides results debugging across the entire Calibre product line, giving you a single interface to learn and support for all your Calibre tools.
- **Reliability:** With thousands of users worldwide, the Calibre RVE interface sets the standard for debug reliability and accuracy.
- **Schematics:** Visualizing the intended connectivity of the source schematic against the connectivity realized in the layout greatly speeds resolution of LVS errors.
- **Short isolation:** Identifying a short and quickly verifying a virtual fix interactively significantly improves designers' productivity .

### Calibre RVE Results Viewing Environment: Accelerating Time to Tapeout

While the Calibre® platform's best-in-class engines provide physical and circuit verification results in record time, you still need to fix the identified layout issues before you can tape out. The Calibre RVE™ results viewing environment provides fast, flexible, and easy-to-use graphical debugging capabilities that minimize your turnaround time and get you to "tapeout-clean" on schedule.

### Physical Verification

However complex the rule deck, the Calibre RVE interface can handle it. Even with millions of error results, the Calibre RVE environment provides fast navigation through the layout, while its filtering capability allows you to focus on analyzing and fixing critical errors first. The



Calibre RVE robust viewing and debugging capabilities connect results from all Calibre tools back into your schematic or layout viewing environments for quick design closure.

# Calibre RVE

tabbed viewing format enables you to easily organize data by tiling the display windows side by side. And, because the Calibre RVE interface is designed with a low-memory footprint, you can run it on the same machine you use for your design environment.

The Calibre RVE interface physical verification capabilities include:

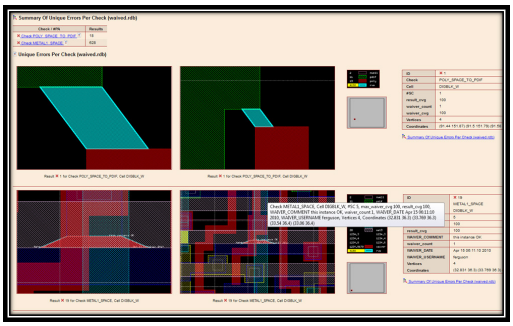
- Automatic display of DRC check-relevant layers in the design environment using the check text override (CTO) file during results highlighting eliminates the need to manually turn on/off design layers, speeding up the DRC debug process
- Filtering capability eliminates clutter and lets designers perform focused debugging
- Interactive results waiving, waiver criteria specification, and waiver export for DRC results provides designers with a full view of all waivers
- Interactive HTML report generation eliminates tedious and time-consuming manual documentation. Designers can automatically record and share information such as waivers, design analysis, sample rules, and final results both internally and externally

**Circuit Verification**

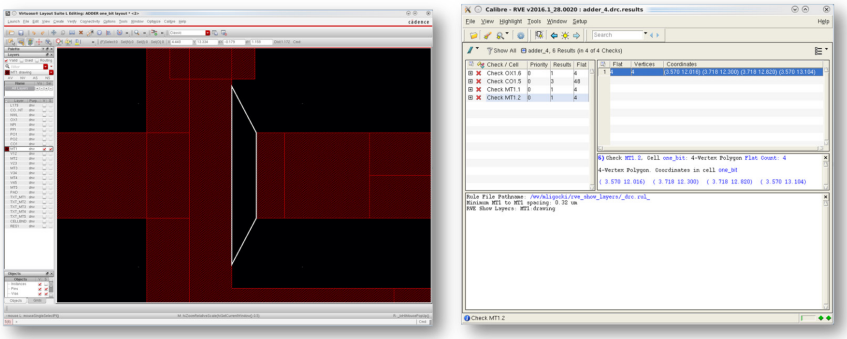
The Calibre RVE interface keeps pace with the expanding requirements of circuit verification using a wide range of capabilities, including: layout vs. schematic (LVS), schematic vs. schematic (SVS), electrical rule checking (ERC), programmable electrical rule checking (PERC), soft checks, voltage-propagation, point-to-point resistance checking, and current density checking. By providing both source and layout schematics, the Calibre RVE interface can easily and quickly cross-highlight between the schematics, the design layout, and the Calibre LVS results report.

Calibre RVE circuit verification capabilities include:

- Fast and intuitive schematic visualization and hierarchical SPICE browser to navigate and highlight nets and devices. Highlights appear in layout and schematic windows, along with the Calibre RVE layout and source schematics.
- Fix suggestions that provide an English description of the error (e.g., “Layout net 5 and 10 are shorted”) to simplify and speed up the debugging process.
- Advanced short isolation function that can be run hierarchically and by layer to quickly isolate the root cause of a texted short. When the short isolation algorithm is unable to pinpoint the short, the Calibre RVE interface enables the user to interactively walk through the shorted-path, isolate the issue, make a virtual fix and confirm the validity of the fix without repeating the batch Calibre LVS run.

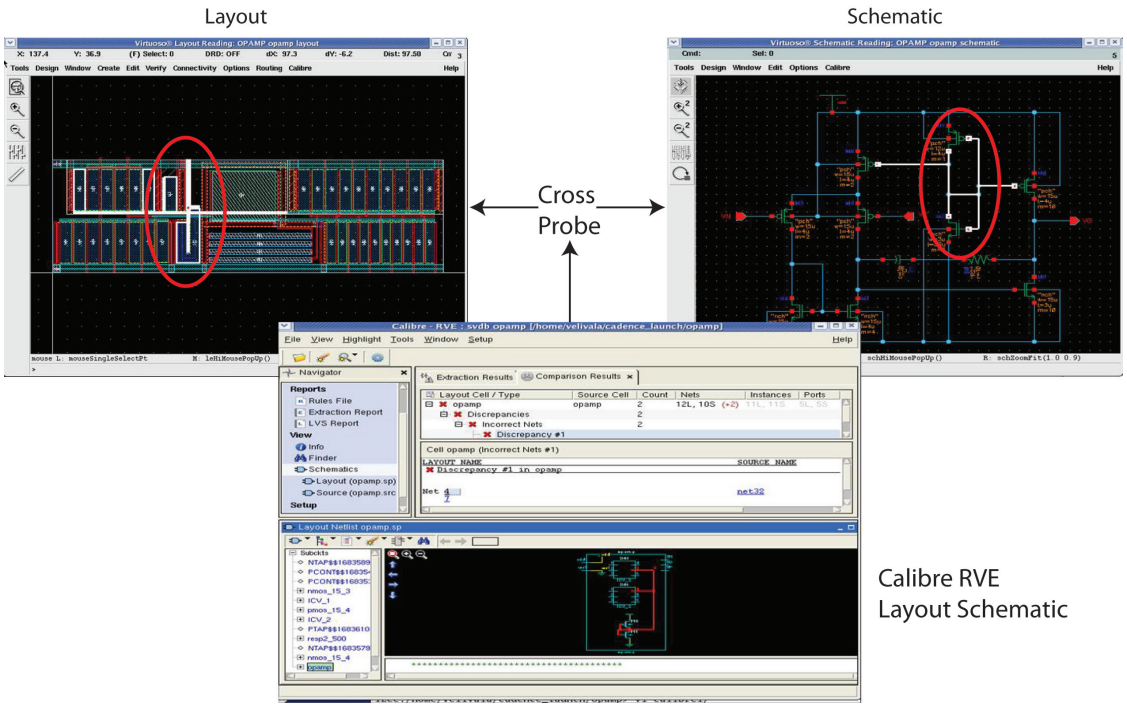


Interactive HTML report generation allows designers to easily document and share design information.



The Calibre RVE interface allows users to automatically display DRC check-relevant layers in the design environment using the CTO file.

**Parasitic Extraction**
Accurate timing and performance simulations for leading edge circuit designs depend on accurate parasitic extraction. Using the Calibre xRC™ and Calibre xACT™ extraction tools with their industry-leading accuracy to extract parasitics from the physical layout ensures high-quality results. The Calibre RVE interface then enables you to quickly and easily navigate those extraction results, and perform both interactive and batch point-to-point calculations.




The Calibre RVE interface offers dynamic cross-probing capabilities between layout, schematic, source netlist, layout netlist, and LVS result files.

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