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Calibre RealTime Digital

Calibre confidence in the digital flow

Siemens Digital Industries Software physical verification

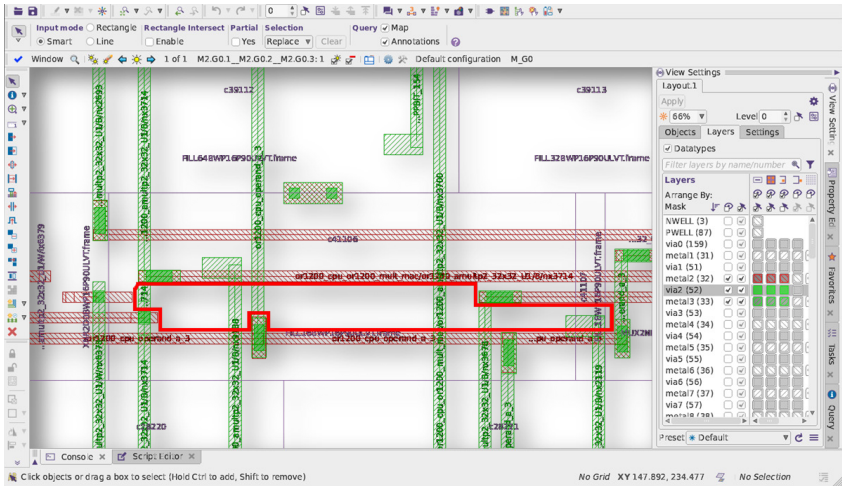
Benefits

- Significantly reduces batch physical verification iterations and overall closure time
- Enables digital designers to perform what-if analysis to optimize designs and/or learn new technology node rules
- Enables digital designers to spend more time achieving PPA goals without impacting schedules
- Supports faster signoff DRC convergence
- Immediate Calibre nmDRC feedback in P&R
- Uses standard foundry-qualified Calibre rule decks
- In-memory checking ensures best performance

Calibre signoff-quality DRC during place & route

The Calibre® RealTime Digital platform enables in-design signoff-quality Calibre design rule checking (DRC) in the digital design implementation environment, providing significant productivity gains for physical design and verification engineers. Using immediate signoff-quality feedback on design rule violations and recommended rule compliance in place and route (P&R) tools, designers can focus on achieving power, performance, and area (PPA) goals without incurring numerous time-consuming design verification iterations. As a result, digital designers can now shave weeks off their tapeout schedule while producing high-quality, optimized layouts.

The Calibre RealTime Digital interface provides direct calls to Calibre analysis engines running foundry-qualified signoff Calibre rule decks. These Calibre engines perform fast, incremental checking in the vicinity of shapes being edited, providing nearly instantaneous feedback on design rule violations, as well as potential systematic variation susceptibility (as measured by recommended rule compliance).



The Calibre RealTime Digital platform completely changes the traditional digital design DRC closure flow by bringing Calibre sign-off quality verification into the P&R environment.

Calibre RealTime Digital

Benefits *continued*

- Built-in error review using toolbar and Calibre RealTime-RVE results viewer enhances ease of use during debugging
- Ability to run all checks or configure custom check recipes
- Uses LEF or GDSII/OASIS views for cells, IP, and memory blocks
- Complements existing built-in native P&R DRC checkers

With its ability to perform all checks that can be run with the Calibre nmDRC™ Platform, including recommended rules, pattern matching, equation- based DRC, preferred metal direction rules, and multipatterning, the Calibre RealTime Digital interface also lets digital designers perform what-if analyses during manual DRC fixing to produce a design that is DRC-clean, resistant to manufacturing variability issues, and optimized for the most desirable performance and operational characteristics. No matter how many DRC errors must be manually corrected, or how complex those checks are, design groups working at the most advanced nodes can get to DRC-clean quickly and with Calibre confidence.

Use models

Digital design DRC closure

Typically, 100s-1000s of DRC errors must be fixed manually in each design, depending on the technology node and design complexity. The Calibre RealTime Digital interface enables physical design and physical verification engineers to quickly validate manual DRC fixes in the P&R environment. A full signoff Calibre batch flow is run initially for reference. Designers then use the Calibre RVE™ interface to highlight and debug batch DRC violations in the P&R tool, and apply the immediate feedback from the Calibre RealTime Digital interface to validate the fixes. Typical Calibre RealTime Digital iterations take a few seconds to a minute, which enables designers to quickly fix 99% of signoff DRC errors with Calibre confidence. By minimizing the number of full-chip verification runs, designers shorten the production schedule when it is most critical—at tapeout.

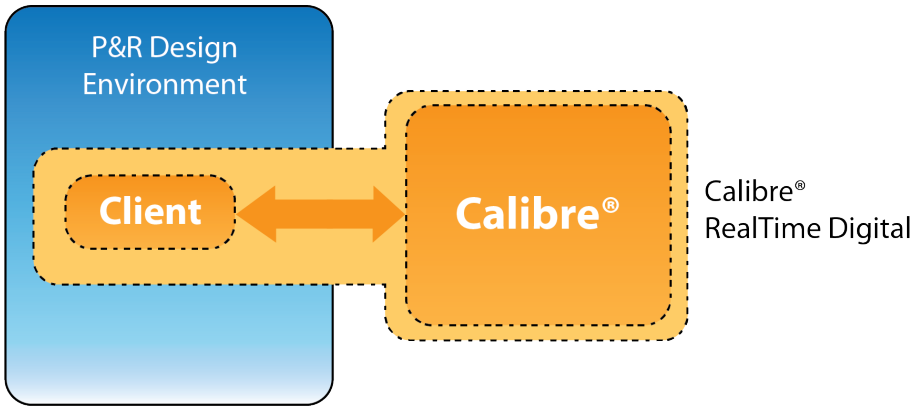
Engineering change orders

Engineering change orders (ECOs) typically generate new DRC errors that must be debugged and corrected manually. With the Calibre RealTime Digital interface, designers can interactively verify windowbased DRC/multipatterning/pattern matching fixes within the P&R environment, using signoff Calibre verification.

Interface DRC errors between top-level and hierarchical blocks

Fixing interface DRC errors is a very iterative process using the conventional DRC verification flow. Merging the GDSII/OASIS for standard cells, intellectual property (IP), memory, and other P&R blocks with the top-level shapes and launching batch DRC is tedious and time-consuming.

The Calibre RealTime Digital interface can intelligently merge only the



The Calibre RealTime Digital interface offers immediate signoffquality DRC to physical design and verification engineers.

required shapes from top-level and hierarchical blocks, launch a DRC run, and highlight both the DRC error marker and the IP shapes around the error marker in the P&R tool. This allows designers to validate the interface DRC fixes without leaving the P&R environment.

Base layer DRC checks during floorplanning

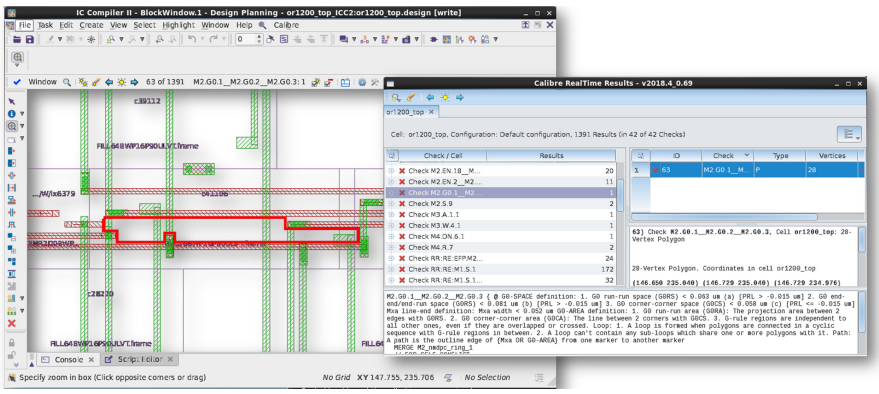
The Calibre RealTime Digital interface enables designers to quickly verify their floorplan and interactively fix base layer DRC errors before delivering the floorplan to the physical implementation team, without the multiple timeconsuming DRC iterations required by traditional flows. Furthermore, the ability to perform base layer signoff DRC augments floorplan checks by supplementing the native P&R tool's floorplan checker with signoff checking.

Interactively learn new technology node rules

The Calibre RealTime Digital interface accelerates the understanding of new design rules through interactive experience. Instead of reading descriptions of complex design rules and checks, digital designers can simply perform a what-if analysis to quickly see and understand the parameters and application of a rule, and identify layout configurations that avoid DRC violations, shortening the DRC closure time. This interactive approach also allows designers to more quickly understand what fixes are needed when a particular DRC error occurs.

Ease of use

The Calibre RealTime Digital interface provides a tight integration between the Calibre physical verification platform and P&R implementation systems. Calibre nmDRC verification is transparently implemented, so users can begin enjoying the advantages of signoff-quality DRC without the usual learning curve.



Designers can highlight results using either the Calibre RealTime toolbar or the Calibre RealTime-RVE window.

The Calibre RealTime Digital interface eliminates any gaps between the P&R tool's built-in design rules and the foundry-qualified Calibre rule deck, so designers know they are getting accurate, up-to-date foundry information at the best possible time—while they are performing manual DRC error fixing during floorplanning and/or tapeout. At the same time, because it is integrated in addition to the built-in checker, users have the freedom to use either or both checking processes, as desired.

The Calibre RealTime Digital built-in error review toolbar eliminates window clutter and enhances ease of use for P&R engineers. Designers can also use the Calibre RealTime-RVE results viewing environment to view all error data, and debug errors in a systematic way based on DRC error type. User-defined custom filters allow designers to create check recipes that limit which checks are run (based on design requirements and organizational processes) without having to modify the foundry-qualified rule deck.

The Calibre RealTime Digital interface enables P&R engineers to spend less time fixing DRC errors, so they can focus on producing high-quality, optimized designs while still meeting ever-tighter production schedules. Because they can now iterate through signoff-quality DRC in the implementation environment, designers can also be confident that the high-performance designs they create will meet all manufacturing requirements.

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