SIEMENS
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Calibre xL

Parasitic Extraction for Inductance

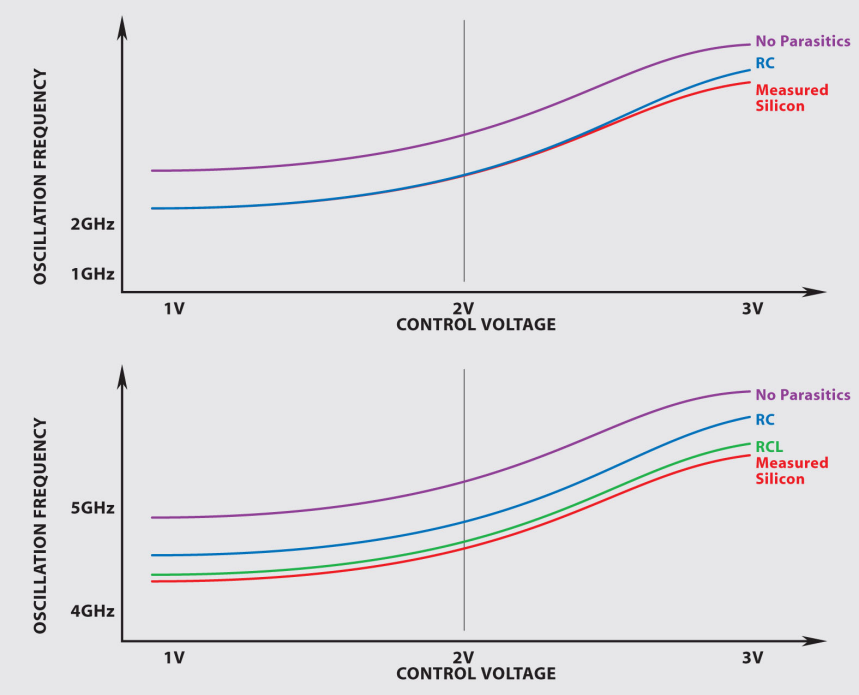
Benefits

- Full-chip, high-performance, parasitic inductance extraction provides highly correlated field solver and silicon-tested accuracyfor analog, RF, and custom digital nanometer designs
- Powerful mutual inductance engine enables extraction of the effect of coupling between different nets
- Parasitic self-inductance extraction integrated with Calibre xRC parasitic RC extraction data enables accurate analysis of high frequency effects in nanometer technology
- Accurate extraction of frequency dependent loop inductance and resistance ensures optimized modeling of on-chip physical effects
- Efficient, realizable model order (RLC) reduction provides manageable netlists and mixedlevel outputs for ease of r e-simulation without loss of accuracy
- Return-path selection and netbased extraction frequency selection offers increased flexibility in performance and improved accuracy
- Seamless invocation, and integration to Calibre LVS, xRC, xACT 3D, and RVE, through Calibre Interactive enables cross-probing and debugging of results in popular layout environments.

Managing Inductive Effects in Nanometer Designs

With increasing operating frequencies, interconnect lines begin to exhibit inductive effects that can significantly influence chip behavior and performance. Parasitic on-chip inductance extraction is crucial for accurate physical verification (simulation) and timely tape-out of high-frequency RF, mixed-signal, and custom digital nanometer designs.

Calibre® xL offers designers full-chip, fast, and accurate extraction of frequencydependent loop inductance and loop resistance, and automatically accounts for return path change with frequency. Results of Calibre xL extraction highly



Parasitic inductance (noise, distortion, impedance mismatch and jitter) can cause chip failure if not accounted for in parasitic extraction. At higher frequencies, inductance can shift the frequency of oscillation in a VCO (lower graphic) and must be taken into account. Parasitic inductance (noise, distortion, impedance mismatch and jitter) can cause chip failure if not accounted for in parasitic extraction. At higher frequencies, inductance can shift the frequency of oscillation in a VCO (lower graphic) and must be taken into account.

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correlate with field solvers and have silicon-tested accuracy.

Calibre xL Inductance Solution
On-chip inductance modeling is challenging because inductive couplings are long-range, and the return paths for the current are frequency-dependent and difficult to determine or predict. A partial inductance approach, which does not require knowledge of the current return path, results in prohibitively large and dense inductance matrices for any reasonable size design and produces netlists that are unmanageable for today's dynamic simulators.

The Calibre xL inductance calculation engine has a unique, accurate, and efficient way of calculating self-loop inductances in complex designs. Automated reduction of model order reduces parasitic R, C, and L data and produces a passive, realizable network for easy and efficient simulation, with no significant loss in accuracy.

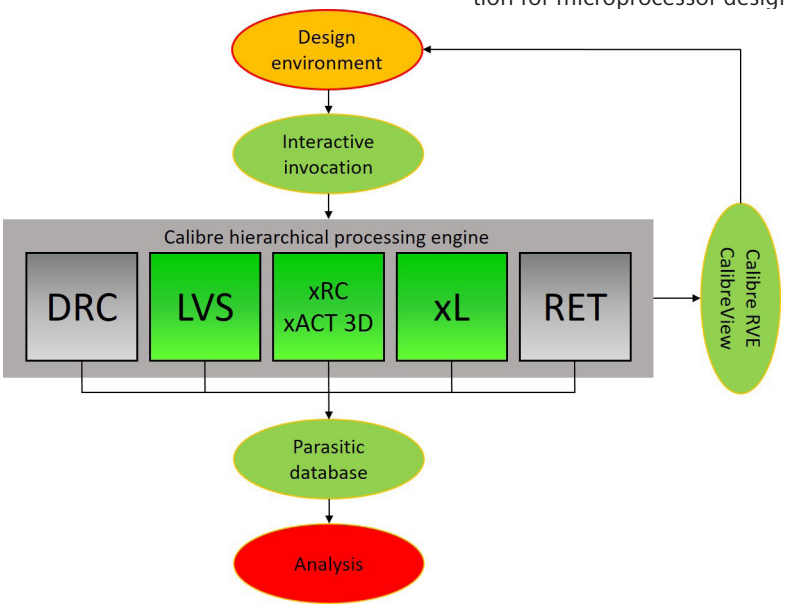
The Calibre xL filtering engine eliminates inductively unimportant wires from the inductance extraction flow, additionally improving accuracy and simulation performance. Its powerful mutual inductance engine allows the designer to extract the effect of coupling between different bundles. The use model for this feature is victim-based, meaning that only victim nets are selected, and Calibre xL then automatically finds the aggressors within a specified area.

Calibre xL offers unprecedented flexibility through selected net extraction, automatic and customizable selection of the return path, net-by-net base frequency selection, and single run multiple frequency inductance extraction, with no need for calibration. Calibre xL has the performance to handle full-chip extraction for microprocessor designs, and the accuracy for analog/RF designs.

Calibre Design Platform and Flow Integration
Calibre xL is fully integrated into the Calibre flow and with popular design environments. It offers designers inductance extraction independent of design style and flow. For analog/RF blocks, it provides necessary accuracy; for digital designs, it provides high capacity and performance.

Calibre xL extends the capability of Calibre xRC and Calibre xACT 3D, the full-chip, industry-proven parasitic extraction solution from Siemens EDA. By reading Calibre LVS data structures directly, Calibre xRC or Calibre xACT 3D works with Calibre xL to provide complete circuit netlist information integrated to the source schematic for back-annotation.

Supported Platforms
32- and 64-bit Linux Redhat and Sun Solaris.



Calibre xL is fully integrated with Calibre LVS, xRC, and xACT 3D for complete circuit netlist information and back-annotation.

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