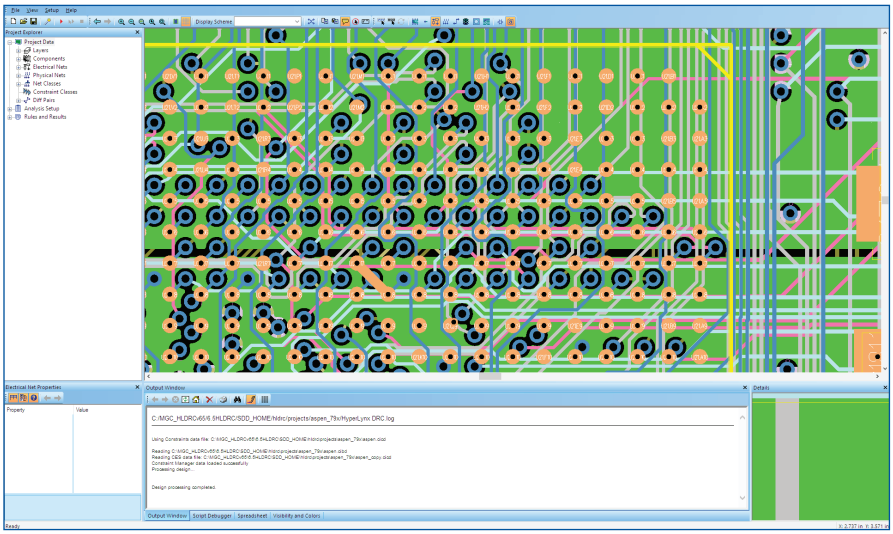
HyperLynx DRC
Standard and Developer Editions

HyperLynx

D A T A S H E E T



Perform design rule checks on boards for electromagnetic interference and signal integrity issues with HyperLynx DRC.

Overview

HyperLynx® DRC is a powerful, fast, electrical design rule checking tool that automates the verification process and enables you to perform design inspection iteratively. Helping you go beyond the error-prone manual approach and limited-scope DRCs built into layout tools, HyperLynx DRC performs complex checks that are not easily simulated, such as rules for traces crossing splits, vertical reference plane change, and EMI/EMC.

The built-in DRCs can be parameterized by PCB designers and hardware engineers alike, as per technology and/or corporate routing or electrical guidelines. Its intuitive Project Setup Wizard makes design setup, rule running, and design analysis easy, irrespective of experience levels. With support for layout data from Mentor and non-Mentor printed circuit board (PCB) design flows, along with ODB++ and IPC-2581 standards, HyperLynx DRC fits seamlessly into your existing PCB process.

With the HyperLynx DRC Developer edition, you can write and execute custom rules to increase coverage of design verification. Database objects such as traces, vias, etc. can be accessed using automation object models (AOM). HyperLynx DRC Developer contains a script writing and debugging environment and supports custom rules and scripts written in JavaScript or VBScript.

What's Included

With 32 built-in Design Rule Checks (DRCs) for items such as relative delay and length matching, via-to-via isolation, and closed trace/return loop, the

FEATURES AND BENEFITS:

- 32 (HyperLynx DRC Standard) and 40 (HyperLynx DRC Developer) comprehensive SI, PI, and EMI/EMC checks
- Rule parameters can be edited based on technology or on corporate or IC vendor guidelines
- Advanced geometric and topological engines for efficient design rule checking
- Easy design setup and navigation
- Cross-probe to location of design violation from Sharelist (HTML format) error report
- Write and execute custom rules with HyperLynx DRC Developer
- Custom rule authoring supports JavaScript and VBScript and rule debugger (HyperLynx DRC Developer)
- Supports layout data from Mentor and non-Mentor PCB flows, including ODB++ and IPC-2581 standards.

HyperLynx DRC Standard edition lets you quickly and easily pinpoint trouble spots in your design that can cause potential signal integrity (SI), power integrity (PI), and electromagnetic interference and compliance (EMI/EMC) issues.

The HyperLynx DRC Developer edition includes eight additional DRCs, such as differential pair symmetry, decoupling capacitor coverage, and acute angle, for a total of 40 rules designed to increase the scope of design verification.

Built-in engines for geometric calculation, path finding, and net topology extraction, along with a 2D field solver, provide quick and accurate results without the need to prepare device models. With the HyperLynx DRC Developer edition, JavaScript or VBScript can be used to access database objects using automation object models and then write and execute custom rules.

Easy Setup and Navigation

HyperLynx DRC is designed for quick and easy access to design data. A built-in Project Setup Wizard walks you through the steps for running design checks on your board. Items such as electrical model assignment, connector definition, power/ground net definition, discrete components, and electrical net definition are all in the Project Setup Wizard.

The scope of the checks can be defined with a specific list of design objects (e.g., power nets, capacitors) called an Object List. With a sophisticated filtering system, a specific object list with names, component values, part numbers, or any other property can be generated automatically.

In addition, the associated parameters for each rule can be edited based on technology and/or corporate guidelines.

		Rule	Standard	Developer
SI	classic	Impedance	◆	◆
	classic	Edge rate	◆	◆
	classic	Guard trace	◆	◆
	classic	Long nets	◆	◆
	classic	Long stub	◆	◆
	classic	Many vias	◆	◆
	classic	Termination	◆	◆
	classic	Crosstalk coupling	◆	◆
	classic	Edge rate to Period	◆	◆
	classic	Topology -Star	◆	◆
	classic	Via stub length	◆	◆
	classic	Via to via isolation		◆
	classic	Acute angle		◆
	DDR	Topology -T folk	◆	◆
	DDR	Topology - Fly-by	◆	◆
	DDR	Delay and Length Matching	◆	◆
	DDR	Relative Delay and Length Matching	◆	◆
	Diff pair	Differential impedance	◆	◆
	Diff pair	Diff pair	◆	◆
	Diff pair	Diff pair symmetry		◆
	Diff pair	Diff pair phase matching	◆	◆
	Diff pair	Diff pair pad parasitic capacitance		◆
	Diff pair	Diff pair spacing		◆
PI	AC	Decap placement	◆	◆
	AC	Decap coverage		◆
	AC	Decap order	◆	◆
	AC	Decap via locations		◆
	DC	Power/Ground width	◆	◆
	DC	PDN via count		◆
EMC	EMI	Exposed length	◆	◆
	EMI	IO coupling	◆	◆
	EMI	Closed trace /return loop	◆	◆
	EMI	Edge shield	◆	◆
	EMI	ICs over split	◆	◆
	EMI	Metal island	◆	◆
	EMI	Net crossing gaps	◆	◆
	EMI	Signal supply	◆	◆
	EMI	Net near plane edge	◆	◆
	EMI	Vertical Ref plane change	◆	◆
	EMI	Filter placement	◆	◆
Any custom rules				◆
Total number of rules			32	40

Error Reports

Once you've run HyperLynx DRC, an error report such as this list of t-fork topology violations is generated from where you can cross-probe to the location of the design violation. In addition, Sharelist reports (containing the image, violation details, and coordinates) can be generated in HTML for broader team review.

Violation type: T-Fork Topology Violations (10)

N	Description	Net	Actual Value	Required Value	Severity	Status	Rank	Time Stamp	Rule name	Rule parameters	x, y coordinates	Screenshot
1	D0 length violation [Dim/Undim /Clear /Zoomout]	DDR2_ADDR[6] [Clear/Zoomout]	2.1 in	1 in	Error	Unknown	1	3/3/2017 10:45:12 AM	Rules/SI /T-Fork Topology	MaxBranches='2' MaxD0='1 in' MaxTolL='0 mil' MaxTolW='0 mil' ReportViolationOnly='1'	8.317 in, 3.945 in	att26713.jpg
2	#2 branch length matching violation [Dim/Undim /Clear /Zoomout]	DDR2_ADDR[1] [Clear/Zoomout]	7.873 mil	0 mil	Error	Approved	1	3/3/2017 10:45:12 AM	Rules/SI /T-Fork Topology	MaxBranches='2' MaxD0='1 in' MaxTolL='0 mil' MaxTolW='0 mil' ReportViolationOnly='1'	8.872 in, 4.179 in	att26717.jpg
3	#2 branch length matching violation [Dim/Undim /Clear /Zoomout]	DDR2_ADDR[1] [Clear/Zoomout]	7.87 mil	0 mil	Error	ToBeFixed	1	3/3/2017 10:45:12 AM	Rules/SI /T-Fork Topology	MaxBranches='2' MaxD0='1 in' MaxTolL='0 mil' MaxTolW='0 mil' ReportViolationOnly='1'	8.872 in, 4.012 in	att26718.jpg
4	#1 branch length matching violation [Dim/Undim /Clear /Zoomout]	DDR2_ADDR[6] [Clear/Zoomout]	375.6 mil	0 mil	Error	Unknown	1	3/3/2017 10:45:13 AM	Rules/SI /T-Fork Topology	MaxBranches='2' MaxD0='1 in' MaxTolL='0 mil' MaxTolW='0 mil' ReportViolationOnly='1'	9.16 in, 4.142 in	att26719.jpg

Scalable Solutions

HyperLynx DRC is scalable, offering a variety of configurations to meet your needs. The questions in the following table can be used to determine which product is best for you.

Customer need/environment	Free	Gold	Standard	Developer
Number of built-in rules	8	22	32	40
Rule complexity	Entry-level	Basic	Mid-level	Advanced
Licensing type	Subscription	Subscription	Time-based / perpetual	Time-based / perpetual
Need to parameterize rules?	◆	◆	◆	◆
Need to share results with others?	◆	◆	◆	◆
Need to import data from ODB++ or 3rd party?	◆	◆	◆	◆
Working on Windows?	◆	◆	◆	◆
Working on Linux?			◆	◆
Need to open HLDPROJ files?			◆	◆
Need to cross-probe from results to board viewer?			◆	◆
Need the ability to open SRs?			◆	◆
Currently own HyperLynx DRC custom rules?				◆
Need to write corporate/technology rules?				◆

Supported PCB layout systems and formats include:

- Mentor Graphics PADS®, Xpedition®, and Board Station®
- Cadence Allegro®, SPECCTRA®, and OrCAD®
- Zuken CADSTAR®, Visula®, CR-3000/5000/8000 PWS, and Board Designer
- Altium® Designer
- ODB++
- IPC-2581

For the latest product information, call us or visit:

www.mentor.com/pcb/hyperlynx/electrical-rule-check/

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