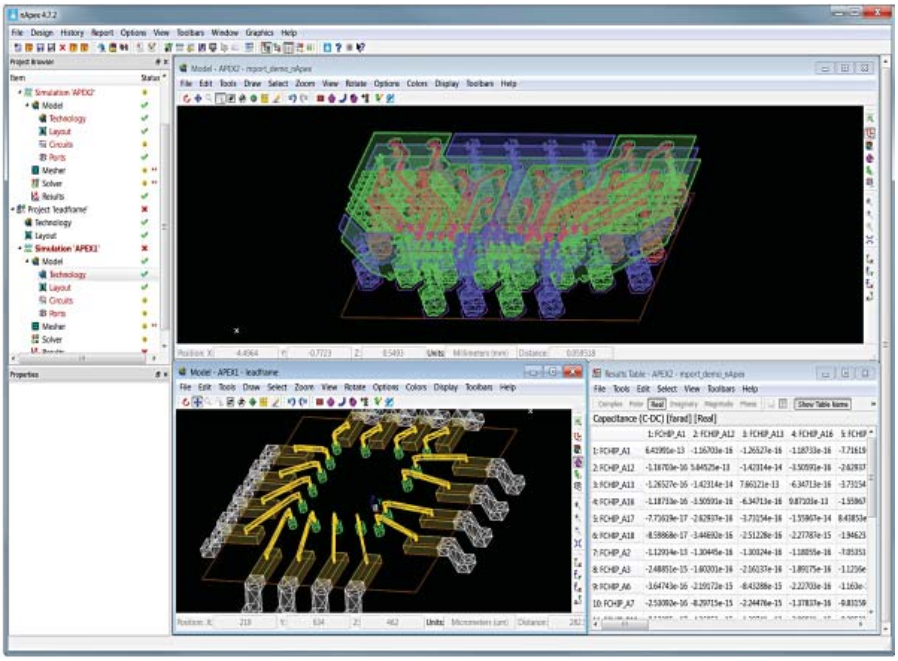
HyperLynx Fast 3D Solver

Accelerated Extraction of SPICE Models for Chip-through-System Design

High Speed Design

D A T A S H E E T



Mentor Graphics HyperLynx Fast 3D Solver is ideally suited for power integrity, low-frequency SSN/SSO, and complete-system SPICE model creation while accounting for skin effect impact on resistance and inductance. The multi-core parallel processing drives extremely fast run times, allowing multiple "what if" scenarios to be run in a minimal amount of time.

FEATURES AND BENEFITS:

- Extreme Accuracy
  - 3D EM solver for all geometries with no reference plane assumptions
  - Broadband model extraction to several GHz
  - High frequency modeling of skin effect for resistance and inductance
- Extreme Performance
  - Fast quasi-static extractor quickly creates full system SPICE netlists
  - Multi-machine parallelization for fast run times
  - Near linear core scaling efficiently uses all CPU resources
- Extreme Usability
  - Easy-to-use; any engineer can perform EM analysis
  - Automation environment inte–grates EM analysis into design flow
  - SI, and PI, modeling available in a single environment

Overview

Mentor Grapics HyperLynx Fast 3D Solver features an accelerated full-3D electro-magneto-quasistatic extractor (EMQS). Designers of chip interfaces, redistribution layers, packages, boards, systems, and SiP, can rapidly and accurately extract SPICE models using the fully automated environment. The solver is ideally suited for power integrity, low-frequency SSN/SSO, and complete-system SPICE model creation while accounting for skin effect impact on resistance and inductance.

Whether the specific application includes high-performance microprocessor design, or low-cost ASIC and system design, the Solver provides effective solutions. It addresses power integrity, signal integrity, and simultaneous switching noise, with its industry-leading ability to handle large designs 20x-100x faster than other equivalent solutions — while maintaining full-3D gold-standard EMQS accuracy. The intuitive GUI enables users working with the latest system-in-package (SiP), package-on-package (PoP), stacked die, and multi-chip module (MCM) scenarios to easily extract accurate models with minimum effort.

With its powerful 3D capabilities, extraction automatically includes handling of power and signal nets with poor references or nets that have significantly different impedances. Additionally, it uses a proprietary loss modeling technique to capture the DC and skin-depth-based high-frequency behavior of resistance and inductance. The broadband behavior is represented by using a single, frequency-independent circuit in the output SPICE model. The deep IP and rich feature set enable users to choose from multiple types of extraction, including impedance, resistance, conductance, capacitance, inductance, and complete SPICE netlists, with or without skin-effect frequency dependence.

Features

3D Electromagneto Quasistatic Extraction

- Accelerated EMQS boundary element technology
- Impedance, resistance, conductance, capacitance, and inductance extraction
- Skin-effect-aware broadband SPICE model generation
- Automatic SPICE model generation
- Choice of L or π model and number of stages in the output netlist
- Volumetric solution for maximum DC accuracy
- Scalable load-balanced multi-core compressed accelerated boundary element technology

Completes Packaging and Analysis Flows

- Integrates directly with Xpedition Package Integrator
- Export models directly to HyperLynx, HSPICE, Spectre, SigXP, Allegro SI, Agilent ADS
- Produces readily-consumed SPICE subcircuits and IBIS package models

Enhanced Usability and GUI Features

- Full scripting capabilities based on Python to completely automate analysis
- Package layout editing and creation
- Flexible model cropping options
- Automated port setup
- Intuitive pin-grouping option
- Chip metal layers, RDL, package, and board merging from industry-standard file formats from Mentor, Zuken, AutoCAD, and Cadence
- PoP, SiP, SoC, MCM, and stacked die support
- Automated refined meshing
- Full 3D control on bond wire, solder ball, solder bump and lead design
- Incorporation of linear passives such as decoupling capacitors directly into the generated model
- Windows and Linux, 64-bit

Performance

- LSF / SGE support for distributed simulation
- Extended large number of cores, multi-core and multi-CPU engine
- Parallel adaptive frequency sweep solving

Applications

- Package-on-package configurations
- Systems-in-package and MCMs
- Coplanar packages
- QFN, QFP, leadframe packages
- Embedded passives
- Detailed via, transition, interconnect, bond-wire, solder ball, and solder bump modeling
- Package and board merged configurations
- Stacked die
- Redistribution Layer (RDL) modeling
- Power distribution networks

For the latest product information, call us or visit: w w w . m e n t o r . c o m / p c b

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