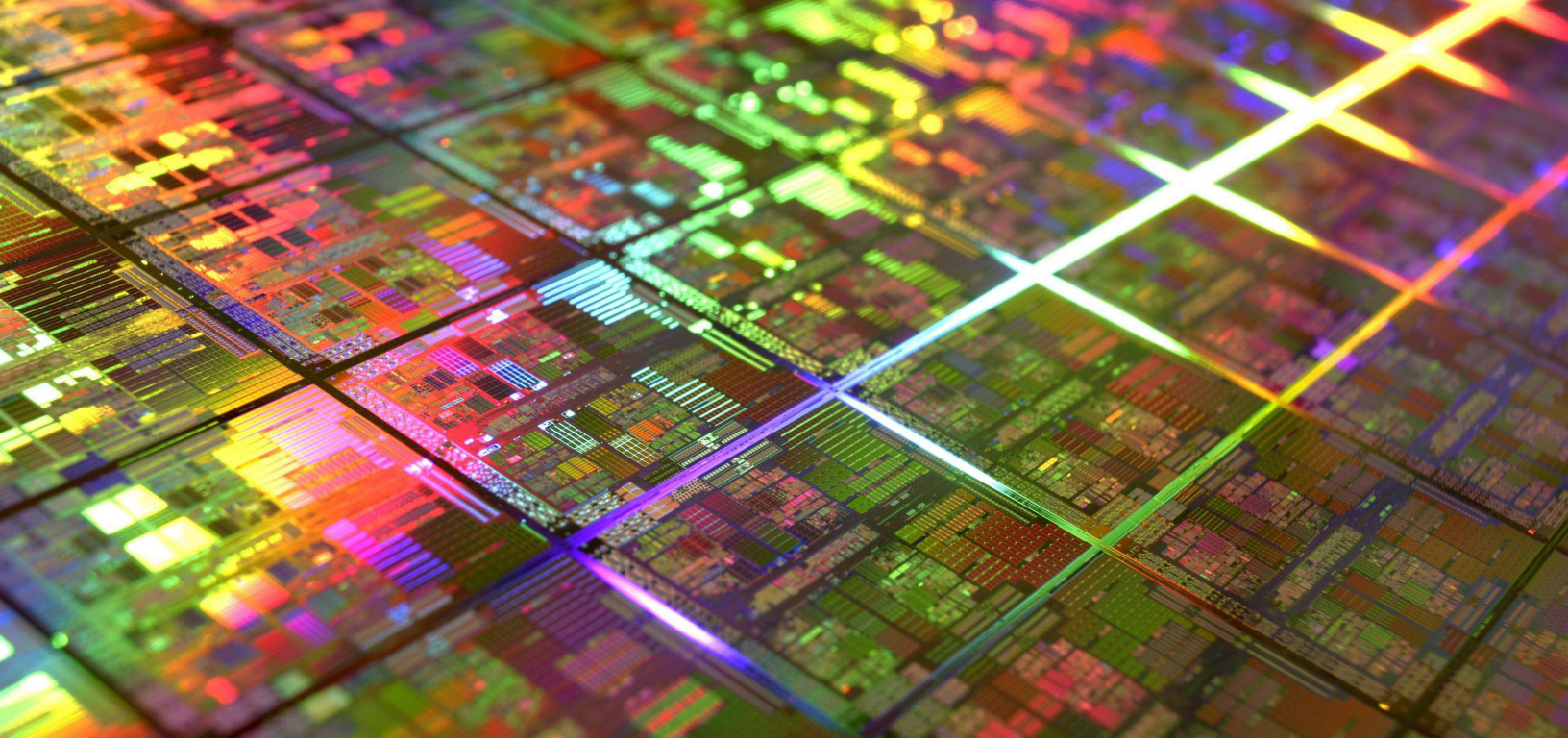

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Questa Design Solutions

Features and Capabilities

Questa Lint

- Static RTL linting capabilities
- Design scoring
- Collaborative team-based debug

Questa AutoCheck

- Automated sequential RTL analysis
- Exhaustive deep bug-hunting capabilities beyond static linting

Questa X-Check

- Automatic X-sensitivity analysis
- Detection of hidden simulation vs. synthesis mismatches

The high impact of design issues on projects

Mistakes happen, but finding and fixing issues late in programs increases overall program scope, as well as schedule and resource requirements. Competitive pressures push teams constantly to do more. Functional verification teams face significant challenges to build testbenches quickly, uncover design issues and enable rapid debug. Incomplete or incorrect bug fixes (or even a hurried introduction of new bugs) compound the problem. In addition, there are classes of design bugs that are challenging to catch at all in functional verification.

Automated intent-focused verification for designers

Efficient, target-adaptable analyses for designers, Questa Design Solutions provides actionable results to enable designers to ensure that their designs meet their intent. These integrated and complementary solutions are built to enable the designer to find issues when they're cheapest to fix, rather than letting them become expensive for the entire project to address. This improves overall team agility through more efficient design processes, as well as by allowing functional verification, emulation, and validation efforts to focus on the hard-to-find functional system issues.

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Features and Capabilities (cont.)

Questa CDC

- Detection of synchronization errors in multi-clock and asynchronous reset designs
- Verification of clock domain crossing (CDC) protocols, including coverage
- Patented metastability models for deep reconvergence verification
- UPF power design-aware CDC verification

Questa RDC

- Detection of design issues across asynchronous reset domains
- UPF power design aware RDC verification

OneSpin Equivalence Checking

- Verification of design equivalence throughout implementation lifecycle

Questa Signoff CDC

- Netlist CDC verification against implementation issues
- Clock, reset and data glitch detection

Questa Design Solutions works with you from design creation through completion with a minimal set of additional inputs. Nothing more than RTL is required, except for UPF and basic constraints, when necessary. All properties and design intent are inferred by the software. Providing common foundations and analysis flows, these solutions enable minimal learning curves to get results between the different analyses. Information specified in an earlier part of the flow is used downstream to ensure consistency and eliminate redundant effort.

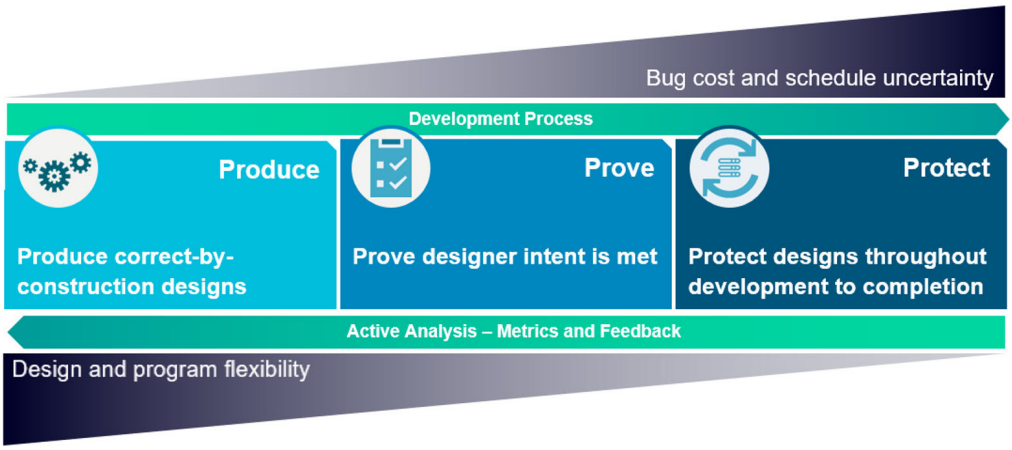
Superior capabilities and quality of results

Through a combination of data analysis, hierarchical and multi-modal technologies, leading analysis engines providing advanced static verification technologies, Questa Design Solutions provides fast analysis with high quality of results and minimal noise. These analyses provide not only results, but insight behind the issues, such as metrics, visualization and recommendations. Questa Design Solutions delivers these results and insights, without a testbench, with technologies built to scale across the most challenging designs and projects.

Benefits and Highlights

Immediate productivity — Questa Design Solutions provide pre-defined configurations for specific methodologies, and within those methodologies, pre-defined development flow-aligned goals to provide out-of-the-box results. With the addition of intelligent inference capabilities, identifying and applying attributes to your design, Questa Design Solutions provide a fast path to finding issues without a lot of setup and configuration.

Data analysis-based assistance — Using proprietary data-analysis techniques, Questa Design Solutions' Assist technologies provide improved setup and configuration, deep root cause analysis and reporting to provide you actionable results and faster fix cycles.



Using only your RTL (and SDC constraints or UPF power intent files), Questa Design Solutions is an integrated and complementary solution that finds and fixes bugs early in the design process when the design and program is still flexible, then preserves the design from unnecessary issues when the cost to address the issue, and the resulting schedule impact, is greater. The solution functions by producing correct-by-construction designs, then proving that the design intent is met and finally protecting throughout the implementation process.

***Scalable solutions* —** Questa's high-performance analysis can process the most complex designs in the industry with unique hierarchical abstraction technologies, and multi-mode analyses,

***Familiar visualization* —** The Design Solutions tools' interfaces are built on the Visualizer UI capabilities, providing familiarity and commonality across Design Solutions tools, and beyond to other Siemens products in simulation, formal verification, emulation and beyond.

***Active analysis* —** Questa Design Solutions are architected to adapt and integrate the insights normally provided later in the development flow, earlier where issues are fastest and cheapest to fix. This adaptive analysis tailors itself for the tasks at hand, to provide focused feedback where and when it's needed most.

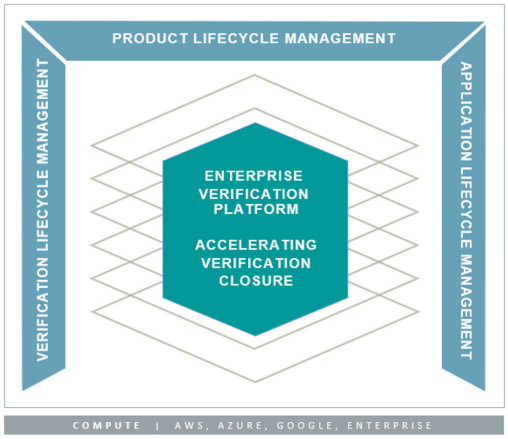
***Traceability support* —** Standards-compliant development flows must exhibit both traceability to requirements and a prescribed level of quality. Some standards require the ability to show the progression of quality metrics over time. Questa Design Solutions products leverage Siemens' long running support of these requirements to deliver these features.

***Continuous integration* —** Questa Design Solutions integrates into popular Continuous Integration management tools, ensuring that throughout the development process, a design, once proven clean, remains that way.

***Verification Management* —** Automatic test plan generation and coverage reporting for analyses enable you to measure the quality of the overall verification, whether via Questa Design Solutions or through simulation, in covering specific design areas of concern.

Enterprise Verification Platform

The Enterprise Verification Platform transforms verification, dramatically increasing productivity and more efficiently managing resources. Questa Design Solutions are integrated with simulation and emulation, sharing common features such as verification management, compilers, debuggers, and language support for SystemVerilog, Verilog, VHDL, UPF, and more. This enables users to select the best application or tool for the job, and then combine results from all the engines to dynamically track the progress of the entire verification program.



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