SIEMENS
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Questa formal applications

Exhaustive solutions from Siemens EDA

Benefits

- **Automated Applications**
  - Each app generates its own assertions, saving hours of work
  - Assertions are generated from automatic RTL DUT analysis and a high-level specification of design intent (CSV, XML, Tcl, or SVA)
  - Because formal analysis is exhaustive, Questa Formal Apps tailored to specific verification tasks are the best tools for those jobs
- **Accelerated Bug Discovery**
  - No need to wait for simulation or UVM testbench bring-up
  - Direct identification of the root cause of an issue via familiar "counter example" waveforms
  - Formal Assertion Libraries for standard protocols
- **Exhaustive Design State Coverage**
  - Not limited by time required to simulate all combinations
  - Not limited by assumptions about what to test for
  - Real-time engine health monitoring

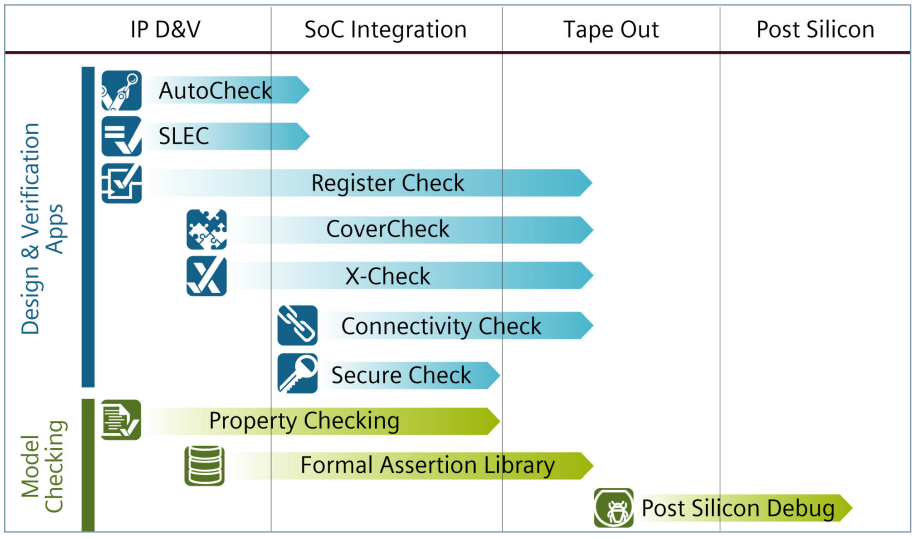
Exhaustive Solutions for Complex Verification Challenges

Even the most carefully designed testbench is inherently incomplete since constrained-random methods cannot hit every corner case. Unfortunately, even after 100% functional coverage is achieved there can still be showstopper bugs hiding in unimagined state spaces. Questa® Formal Apps statically analyze a design's behavior with respect to a given set of properties; then exhaustively explore all possible input sequences in a breadth-first search manner. This uncovers design errors that would otherwise be missed or are impractical to find with simulation-based methods.

Automated Formal Applications

Questa Formal Apps boost verification efficiency and design quality by exhaustively addressing verification tasks that are difficult to complete with traditional methods, and they don't require formal or assertion-based verification experience.

Properties are synthesized from a combination of automatic RTL design analysis and a high-level specification of design intent. The generated properties are then exhaustively verified with formal analysis engines.



Questa formal-based applications offer a broad spectrum of solutions which complement simulation in a number of key areas throughout a project's lifecycle.

Questa formal applications

Benefits *continued*

- **Complements Dynamic Simulation**
  - Exhaustive RTL code unreachability analysis and code coverage closure
  - X-state pessimism and optimism analysis and propagation
  - Supports SVA, PSL, and OVL properties; Verilog and VHDL DUTs
  - Results can be integrated with other Questa flows

The Questa Formal App suite includes applications to address tasks such as: static and conditional connectivity checking, secure path integrity checking, unreachable code identification, X-state propagation, state-space analysis, and register verification. Additionally, the Questa Sequential Logic Equivalence Checking (SLEC) App uses formal methods to perform exhaustive comparisons between inputs to reveal any behavioral discrepancies that could arise in clock gating, ECO integration, re-pipelining, or fault mitigation logic.

Model Checking and Verification IP

In interactive formal model checking, users write properties for assertions (tests), assumes (constraints), and coverage, then run Questa PropCheck to reveal any discrepancies between the specification and DUT. PropCheck supports advanced methods for deep, state-space analysis; such as, abstraction, decomposition, assume-guarantee, goal posting, and waypoints. Model checking can also address issues of interface protocols, functional coverage, control logic, data integrity, and post-silicon debug, which, together, provide the most exhaustive possible analysis of a design. Formal-optimized Verification IP is available for popular standard protocols.

Benefits and Highlights

Automated apps – Questa Formal Apps provide fast, accurate, push-button automatic verification of specific design aspects that are difficult, time consuming, or virtually impossible to verify using traditional methods.

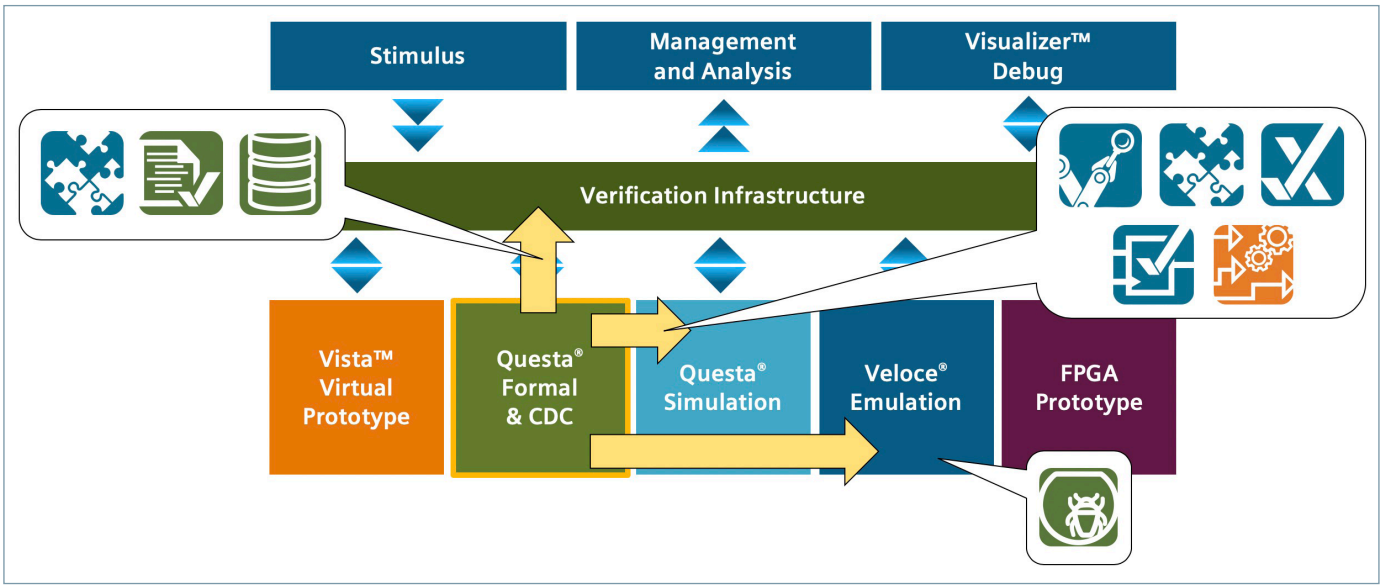
Find bugs early – Questa Formal Apps enable verification to be started early in the design phase, before a simulation testbench is ready.

Improve verification quality – The exhaustive approach enables your analysis to traverse the entire state space, revealing unexpected corner-cases that can be missed by other verification methods.

Increase verification throughput – Use files you have on-hand to automatically generate assertions and run them through the formal engines. These files include the DUT's RTL and task-specific specification files; such as, a CSV file that describes the connectivity of IPs in a SoC or an XML file capturing complex register access policies.

Under-the-hood, Questa Formal's world-class, high capacity, high throughput engines effectively build on their respective strengths by cooperating with each other in real time; thus completing verification faster. Any discrepancies are illustrated with a "counter-example" waveform that shows the root cause of the issue, significantly reducing debug time and effort.

High performance analysis – Dedicated applied research and engineering investment in Questa Formal core technologies have produced continuous improvements in wall clock performance, memory usage, and storage consumption. Together with optimized engines under-the- hood, this means Questa Formal regularly exceeds demanding scalability and compute resource expectations.



An Integral Part of the Enterprise Verification Platform

Built upon several powerful technologies, the Enterprise Verification Platform transforms verification, dramatically increasing productivity and more efficiently managing resources. Sharing a common language front end with Questa and leveraging the IEEE standard Unified Coverage Database (UCDB), Questa Formal solutions are tightly integrated with simulation and Veloce® emulation, sharing common features such as verification management, compilers, debuggers, and language support for SystemVerilog, Verilog, VHDL, UPF, and more. This enables users to select the best application or tool for the job, and then combine results from all the analysis technologies to dynamically track the progress of the entire verification program.

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