SIEMENS
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Questa Visualizer

State-of-the-art testbench debug

Benefits

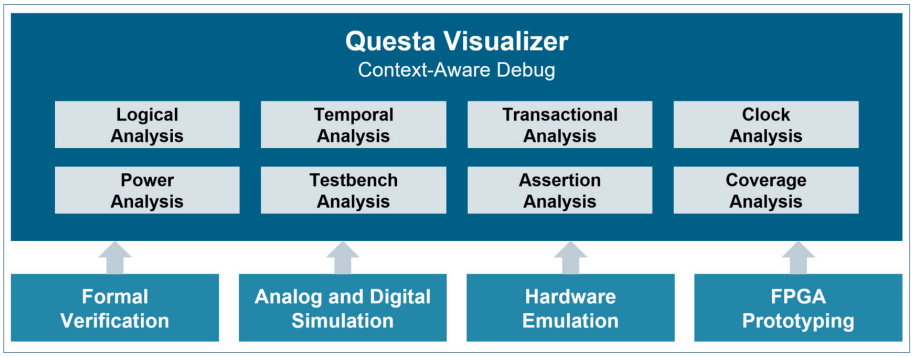
- **Scalable**
  - Compact, efficient waveform database
  - Fast simulation with full visibility
  - On-demand datasets for simulation, emulation, and validation
- **Comprehensive, Easy-to-Use RTL Debug Capabilities**
  - Intelligent root cause analysis with TimeCone view
  - Biometric search for design-wide highlights
  - Intuitive protocol-level debug
- **UVM-Aware Debug**
  - Debug classes in both post and live simulation mode
  - Navigate and debug phase, memory, sequences, threads, factory, locals, and configuration
  - Debug SystemVerilog Assertion with interactive replay
- **Power Aware Debug**
  - Intuitive visualization and overlay of UPF in design context
  - Dedicated tables to visualize source and domain crossings and debug power intent
  - Easy sort and debug of static and dynamic checks
- **Supports Verilog/SystemVerilog, VHDL, and SystemC**

The Changing Landscape of Debug

For years the process of ASIC and FPGA design and verification debug consisted primarily of comprehending the structure and source code of the design with waveforms showing activity over time, based on testbench stimulus. Today, functional verification is exponentially complex with the emergence of new layers of design requirements (beyond basic functionality) that did not exist years ago; for example, clocking requirements, security requirements, safety requirements, and requirements associated with hardware-software interactions. Given these complex interactions, effective debug often demands experts that are familiar with all of the components and a debug environment that is aware of these heterogeneous requirements. According to the 2018 Wilson Research Group Verification study, design and verification engineers now spend almost 40% of their overall project time debugging — and that percentage is growing.

Addressing the Debug Challenge

Questa® Visualizer™ is a context-aware debug platform that supports a complete logic verification flow, including simulation, emulation, and prototyping as well as design, testbench, low-power, and assertion analysis. Visualizer provides a high performance/high capacity debugger that scales from simulation to emulation. Multiple automated features quickly find RTL, gate-level, and protocol bugs. Low- power and UPF debug is fully integrated and overlaid with RTL views. Visualizer is SystemVerilog class-based and UVM-aware to speed up overall debug time, even on today's most complex SoCs and FPGAs.



The Questa Visualizer context-aware debug environment for the Siemens EDA Enterprise Verification Platform

Questa Visualizer

Intuitive User Interface with Powerful Design Debug Features

On top of this intuitive foundation, there are powerful features that elucidate the design and its functionality. These include a TimeCone view, which automates the tracing and visualization of the cause of an event (such as an X) back to its source through multiple clocks, and biometric search, an easy way to search and highlight where a particular value occurs throughout the design.

Unified Debug for Simulation/Emulation

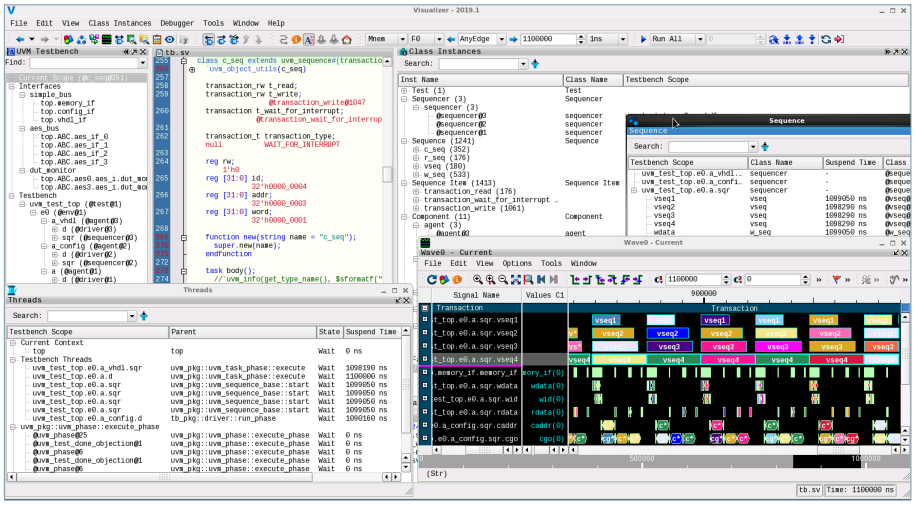
Visualizer delivers high-performance debug through its integration with Questa simulation and Veloce® emulation. Visualizer seamlessly merges UVM data from Questa and design data from Veloce in a single debug cockpit. All advanced debug features (e.g., power) are common across both engines. In addition, Visualizer has an on-demand, incremental design and waveform loading capability so only the required modules, hierarchies, and waveform data for a specified duration of time are loaded. Thus, the debug environment can be dynamically scaled to handle the very large datasets typical in emulation while presenting data on-demand and maintaining very fast start-up times. Integration with Veloce also supports viewing annotation and browsing paths of synthesized logic in the context of the RTL design environment.

State-of-the-Art Testbench Debug

Modern testbenches using the UVM class-based methodology require a debug approach that's more like that found in software development, rather than the time-based RTL and gate- level debug traditionally done by ASIC and FPGA designers. Visualizer offers unique capabilities to view and debug dynamic class member variables alongside DUT signal values in post-simulation and live-simulation modes. The hierarchy browser supports full display of the UVM component hierarchy and enables navigation through the source code with full annotation, so users can easily see testbench values in time. The UVM schematic shows testbench connectivity and the interfaces connecting to the DUT. Visualizer understands and simplifies the underlying UVM internal architecture by presenting just the vital information filtered from the UVM environment.

Unique Advanced Power Aware Debug

Today's design projects actively manage power with a variety of techniques, and various aspects of power- management must be verified and debugged. Power intent is managed with the UPF standard since it cannot be directly described in an RTL model. Visualizer weaves together the information from the UPF and RTL in all design views, including waves and schematics, for a seamless debug experience. Visualizer power aware debug provides a consistent experience across all functional verification engines, and it has the intelligence to quickly provide pointers based on static and dynamic checks.



Visualizer's single environment for class-based testbench and RTL DUT debug.

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