DIGITAL INDUSTRIES SOFTWARE

Veloce proFPGA

A high-performance, easy-to-deploy system for desktop FPGA prototyping

Benefits

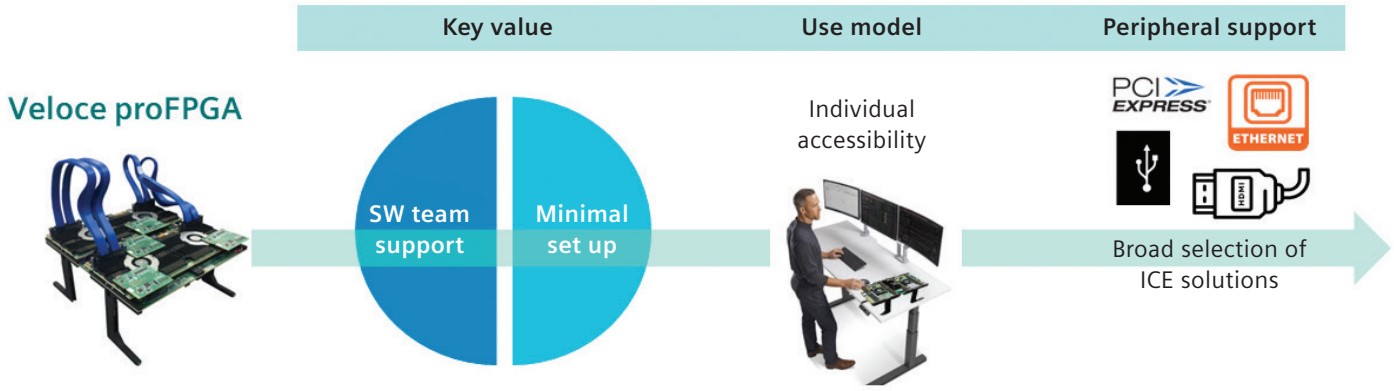
- High performance
- Best-in-class modularity
- Rich availability of FPGA I/Os and SerDes
- Timely support for new FPGA devices
- Most compact prototyping system
- Fast bring-up and easy-to-use

Summary

The Veloce™ proFPGA system architecture offers best-in-class modularity, scalability, flexibility and portability to serve the verification requirements of today's hardware and software engineers. Veloce is a part of the Xcelerator™ portfolio, a comprehensive and integrated portfolio of software and services from Siemens Digital Industries Software.

Veloce proFPGA

The Veloce proFPGA platform offers three types of motherboards: Uno, Duo and Quad. These motherboards allow different types of field-programmable gate array (FPGA) modules to be easily plugged and mixed as well as peripheral memory and protocol interface boards. As a use case example, the engineer can start with the proFPGA Uno system for IP or sub system on a chip (SoC) development and can reuse it for the complete SoC and application-specific integrated circuit (ASIC) prototyping. This is done by simply plugging in the same Veloce proFPGA modules from the Uno on a Duo or Quad motherboard regardless of the type of FPGA used on the new systems.



This innovative and smart mixing technology offers maximum reusability and highest return on investment because the new Veloce proFPGA modules based on the latest FPGA devices are compatible to previous Veloce proFPGA generations. The user can reuse all existing proFPGA motherboards, FPGA modules, daughter cards and accessories in combination with the new Veloce proFPGA modules and systems. If capacity needs to increase with the evolution of the SoC, it is possible to easily connect 14 Veloce proFPGA Quad systems to scale it to an even larger system with a capacity well above the one billion ASIC gates.

Capabilities

Verification environment

The scalability, modularity and flexibility of Veloce proFPGA allows users to expand the prototype solution's verification reach, adding extension boards for memory modeling and hardware interfaces to the external system.

Nearly all FPGA I/Os are available on a rich number of extension sites, which are used for the FPGA-to-FPGA high speed interconnections or for connecting extension boards such as memory, protocol interfaces and application-specific boards. This way, the user can model the Veloce proFPGA system to meet their design verification requirements and scale the system capacity up in a very easy way, if required.

This architectural approach offers maximum flexibility and IP capacity for in-circuit interconnections and for adapting off-the-shelf proFPGA daughter boards for PCIe Gen3/4/5 DDR4 memory, USB3, QSFP+, MIPI, HDMI, SATA, Gigabit Ethernet, debug interfaces or the user's application-specific extension boards.

Solid software solution

The same software flow that accelerates the setup of the Veloce Strato+ emulation platform and the Veloce Primo enterprise prototype is now brought as an option to engineers for accelerating the bring-up of their desktop prototype solution Veloce proFPGA. The Veloce OS for Veloce Prototyping Software (VPS) is a complete automated software that removes tedious tasks to ensure the proper functionalities at the maximum possible speed of the FPGA prototype solution.

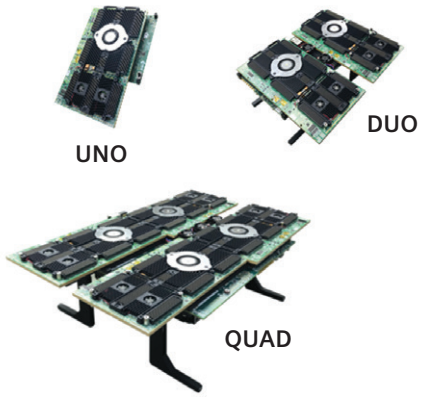
On top of the synthesis frontend process, the software guarantees that the clock tree is properly mapped on the FPGA reconfigurable logic, gated clocks are well propagated, timing hazards are avoided, the memories are automatically inferred and mapped on the available physical memories on the system and the timing constraints are met for maximizing performance without encountering timing violations in the circuit under test. Partitioning of the design across multiple FPGAs is timing-driven and efficient in resources with the user in control of resource versus performance trade-off decisions. Users can direct as much or as little of partitioning as needed to achieve runtime performance objectives. Mapping the design into FPGA resources delivers a high quality of results (QoR), enabling single FPGA designs or logic blocks within one FPGA to achieve 150+ MHz performance.

Advanced debug capabilities

VPS delivers the industry's best prototype debug capabilities, regardless of the prototype's use model and environment. For in-circuit verification (ICE) environments, VPS delivers broad and deep, probe-based, at-speed debugging. Tens of thousands of signals per clock domain can be instrumented at compile time, with runtime selection of the trace set, conditional capture, trigger conditions and events. Many seconds of runtime can be captured by streaming trace data to memory or disk without the need for additional hardware set up and configuration.

Summary

Veloce proFPGA dramatically lowers the adoption barrier of the FPGA desktop prototype solution. Together with the performance that



is possible to reach thanks to its architecture innovations, the solution is easy to deploy and engineers can now bring-up on their own lab environment quickly and reliably.

Veloce proFPGA is based on the latest high-end FPGA from Xilinx and Intel. It has been designed for high performance and the choice of one FPGA per module architecture approach. The solution offers the required modularity for expanding the capacity as needed as well as providing sufficient I/O connections for connecting the interface boards required for creating the verification workload specific to the target application.

The flexibility of Veloce proFPGA allows the user the possibility to use the desktop prototype within various types of workloads, with onboard testbenches and in-circuit connections to external hardware as Ethernet generators or PCI Express buses. For bring-up of the design under test on the prototype, the Veloce proFPGA desktop prototype solution shares the same software frontend as the other solutions in the Veloce hardware-assisted verification system to ensure continuity on the methodology.

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