DIGITAL INDUSTRIES SOFTWARE

QuestaSim

Benefits

- Industry-leading high performance multi-language simulator
- High-performance, high-capacity unified debug
- Reference simulator for LRM compatibility
- UVM, SystemVerilog, VHDL, SystemC, and mixed language support
- Native compiled, single kernel simulator technology
- Next generation Visualizer debug environment
- Code coverage and functional coverage
- SVA and PSL assertions
- Intelligent coverage closure

Sophisticated SoC verification

The QuestaSim™ verification solution from Siemens EDA, a part of Siemens Digital Industries Software, continues to evolve in response to the growing complexity of SoC designs. In addition to the sheer size of designs and the inclusion of multiple embedded processors and advanced interconnect systems, the increase in software content and the configurability required by multi-platform design require a functional verification solution that unifies a broad arsenal of verification features. This places tremendous importance on having a verification plan informed by the collection of coverage metrics that track progress against the plan throughout the verification process. This intelligent verification plan enables engineers to allocate and manage resources efficiently and identify trends as the project progresses.

QuestaSim's powerful technologies help to maximize the effectiveness of your verification at the block and subsystem levels, so your system-level verification can focus on system-level functionality, including software, without having to worry about lower-level bugs eating away at your productivity. No one wants to compromise product quality. However, time-to market pressures dominate SoC projects. To deliver quality within schedule requires shortening the time to achieve coverage and quality goals and improving debug productivity.

Benefits *continued*

- Integrated verification management and analysis
- Simulate in advanced optimization mode
- Best-in-class power-aware verification technology
- Profiling for hotspot analysis
- C code debug
- X-propagation dynamic simulation
- Real number modeling (RNM)
- Common coverage database and flows
- 64-bit support for Linux and Windows

Platform support

- QuestaSim supports Windows and Linux (both 32 bit and 64 bit)
- Windows 10, Linux RHEL 7 and 8, ARM64, Linux SLES 12 and 15 *

The QuestaSim simulator achieves industry-leading performance and capacity through very aggressive, global compile and simulation optimization algorithms for SystemVerilog, VHDL, and SystemC. With unique capabilities for pre-optimization and reuse, QuestaSim supports very fast turnaround times and effective library management while maintaining high performance, thus enabling dramatic regression throughput improvements when running a large suite of tests. The Questa Visualizer debug environment provides high-performance, high-capacity debugging, enabling dramatic regression throughput improvements when running a large suite of tests.

Advanced optimization and productivity flows

QuestaSim supports advanced optimization algorithms designed to significantly improve simulation performance. To improve compilation, optimization, and elaboration turn-around times, QuestaSim supports: a single compile command wrapper called Qrun that automatically provides incremental compile, the ability to save and reuse pre-compiled parts as preoptimized design units (PDUs) and save and reuse elaboration images. These features can be used individually or in combination to provide customized flows that reduce turn-around times by removing unneeded reprocessing.

Code coverage and functional coverage

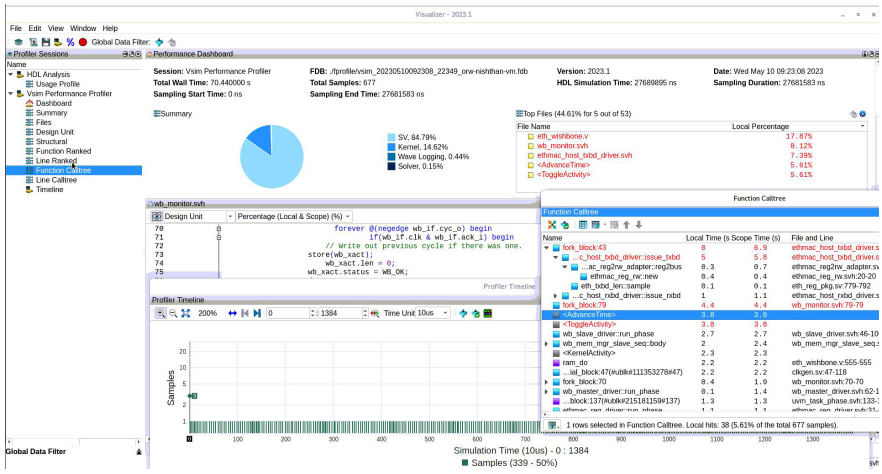
Design verification completeness can be measured through code coverage and functional coverage. QuestaSim supports statement, expression, condition, toggle, and FSM coverage. Code coverage metrics are automatically derived from the HDL source. Because many design blocks are configurable and reusable and not all metrics are valuable, code coverage metrics can be flexibly managed with source code pragmas and exclusions specified in the code coverage browser.

Verification management

QuestaSim verification management and coverage handles data complexity, guides the verification process, and provides automation across all verification engines. This improves verification productivity and performs native generation of coverage data for use in Siemens' industry-leading, next-generation analytics suite: Questa Verification IQ. QuestaSim Verification IQ offers analysis and optimization features built upon the Unified Coverage Interoperability Standard Database (UCISDB), providing results and trend analysis, test plan tracking, and run management. QuestaSim verification management efficiently ties all verification-related tasks together and gives all parties — system architects, software engineers, designers, and verification specialists — real-time visibility into a project. This visibility helps to hit market windows on schedule, manage risk, and improve throughput and debug turnaround times.

Run-time performance profiling

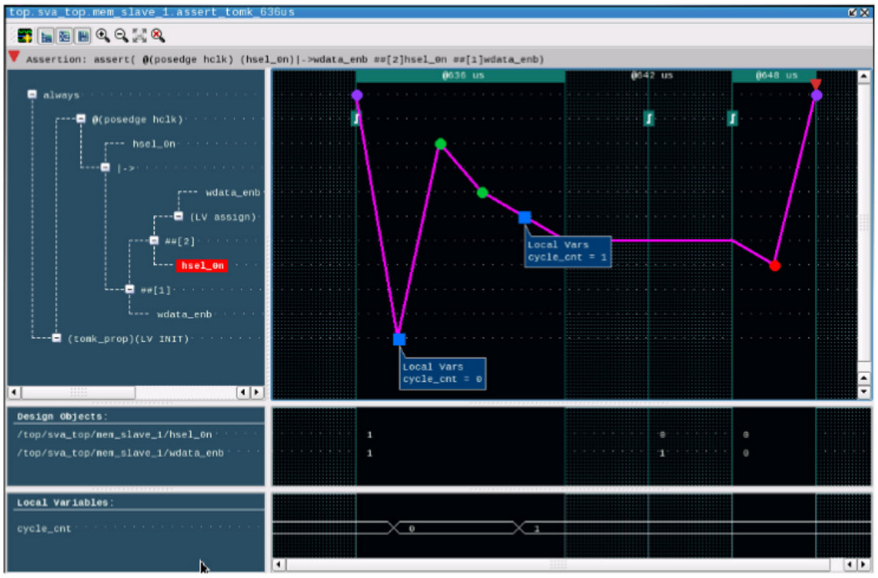
Maximizing the efficiency of RTL verification often requires analyzing simulation run-time performance to look for bottlenecks and potential improvements. QuestaSim's new, completely re-architected and intuitive performance profiler helps users self-diagnose performance bottlenecks by highlighting inefficiencies in the design or testbench that are sub-optimal and can be fixed.



The QuestaSim intuitive performance profiler.

Assertion-based verification with SVA and PSL

Assertion-based verification (ABV) improves design quality through the insertion of white-box monitors that allow active monitoring of functional correctness within the Visualizer debugger window. Assertions catch errors that tests activate but fail to propagate to typical black-box observation points, such as the primary outputs. The assertions also turbocharge time-to-debug productivity because they identify functional bugs much closer to the root cause. The time savings from a significantly shorter causality traceback can reach hours or even days. QuestaSim enables ABV through support of SystemVerilog Assertion (SVA) constructs and the Property Specification Language (PSL). Both SVA and PSL assertions can be either embedded within the design HDL source code or specified in separate units, then bound to the appropriate module instance in the design hierarchy. QuestaSim also offers power debug capabilities with the assertion thread viewer.

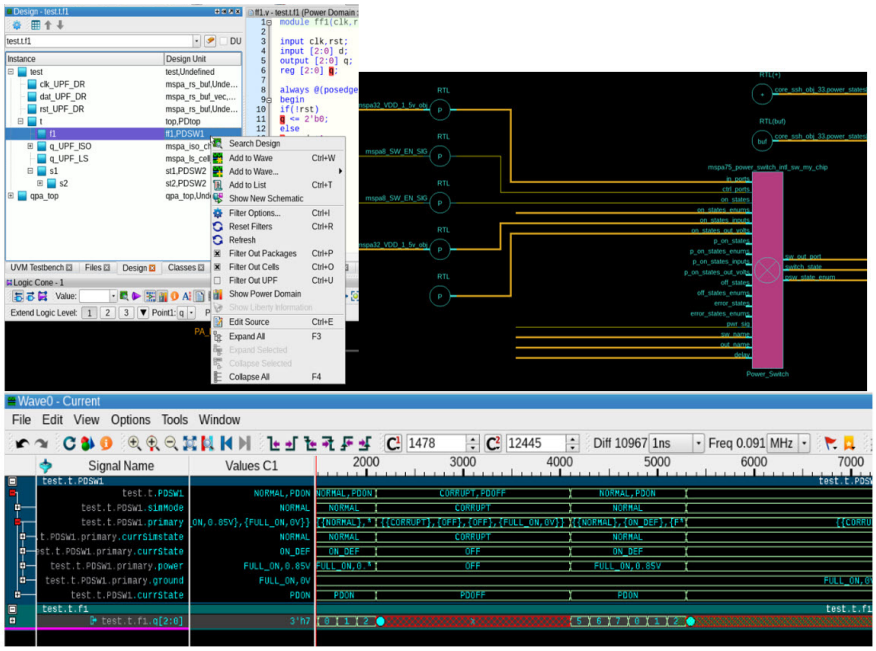


Assertion thread viewer in Visualizer.

Power-aware verification

QuestaSim low-power verification enables early verification of active power management at the RTL, even for the most complex designs. This ensures that the power management architecture and behavior are correct and that the design will operate correctly during active power management. The best-in-class QuestaSim PowerAware technology simplifies the verification process through a comprehensive suite of static checkers, for checking the consistency of the power management architecture, and dynamic checks, for automated error detection. The QuestaSim PowerAware tool also provides visualization of power management architecture and behavior, coverage data collection, and test plan generation for power states and state transitions.

Based on the latest industry standard IEEE 1801, QuestaSim PowerAware supports UPF 3.1 and all UPF 3.0/2.1/2.0 UPF specifications for active power management. The QuestaSim PowerAware solution integrates well with other UPF-based tools to support multi-tool and multi-vendor low power design and verification flows.



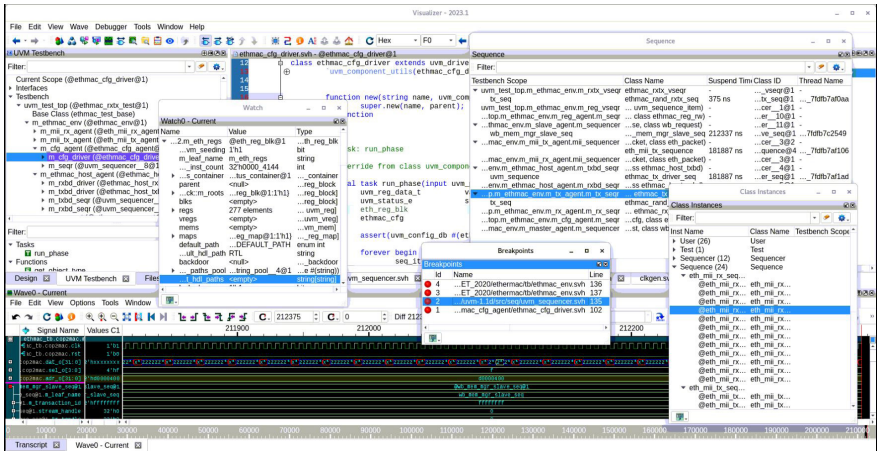
Advanced power-aware debug in Visualizer.

X-Propagation

One of the major challenges in simulation is X-propagation. Determining the sources of propagated Xs requires more time to debug late in the verification cycle, as engineers must identify the sources of Xs, test the initialization of the design, and create explicit checks to report Xs. Questa Xprop dynamic simulation consists of mechanisms to handle the propagation of Xs. It ensures simulation closely matches the silicon behavior, traps the source of Xs during simulation, and ensures signals resolve to a known value if possible.

Real number modeling

QuestaSim supports real number modeling. Real number modeling enables better modeling of analog blocks and allows these discrete models to be used in a high-performance digital flow.



Visualizer's single environment for testbench and RTL DUT debug.

Next generation debug – Questa Visualizer

Questa Visualizer is a context-aware debug platform that supports a complete logic verification flow, including simulation, emulation, and prototyping, as well as design, testbench, low-power, and assertion analysis. It has intuitive features with powerful design and verification debug capabilities for debugging in live-sim mode or post-sim mode. Visualizer provides a high-performance and high-capacity debugger that scales from simulation to emulation. Multiple automated features quickly find RTL, gate-level, and protocol bugs. Low-power and UPF debug is fully integrated and overlaid with RTL views. Visualizer is SystemVerilog class-based and UVM-aware to speed up overall debug time, even on today's most complex SoCs and FPGAs.

Further resources

- Siemens EDA verification expertise provides resources and sample designs to help you get started adopting advanced verification techniques.
- For a collection of free online courses and resources, focusing on key aspects of advanced functional verification go to The Verification Academy.
- To reach solution-driven consultants that dramatically reduce your verification process times while improving quality, check out Siemens EDA Consulting Verification Services.

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