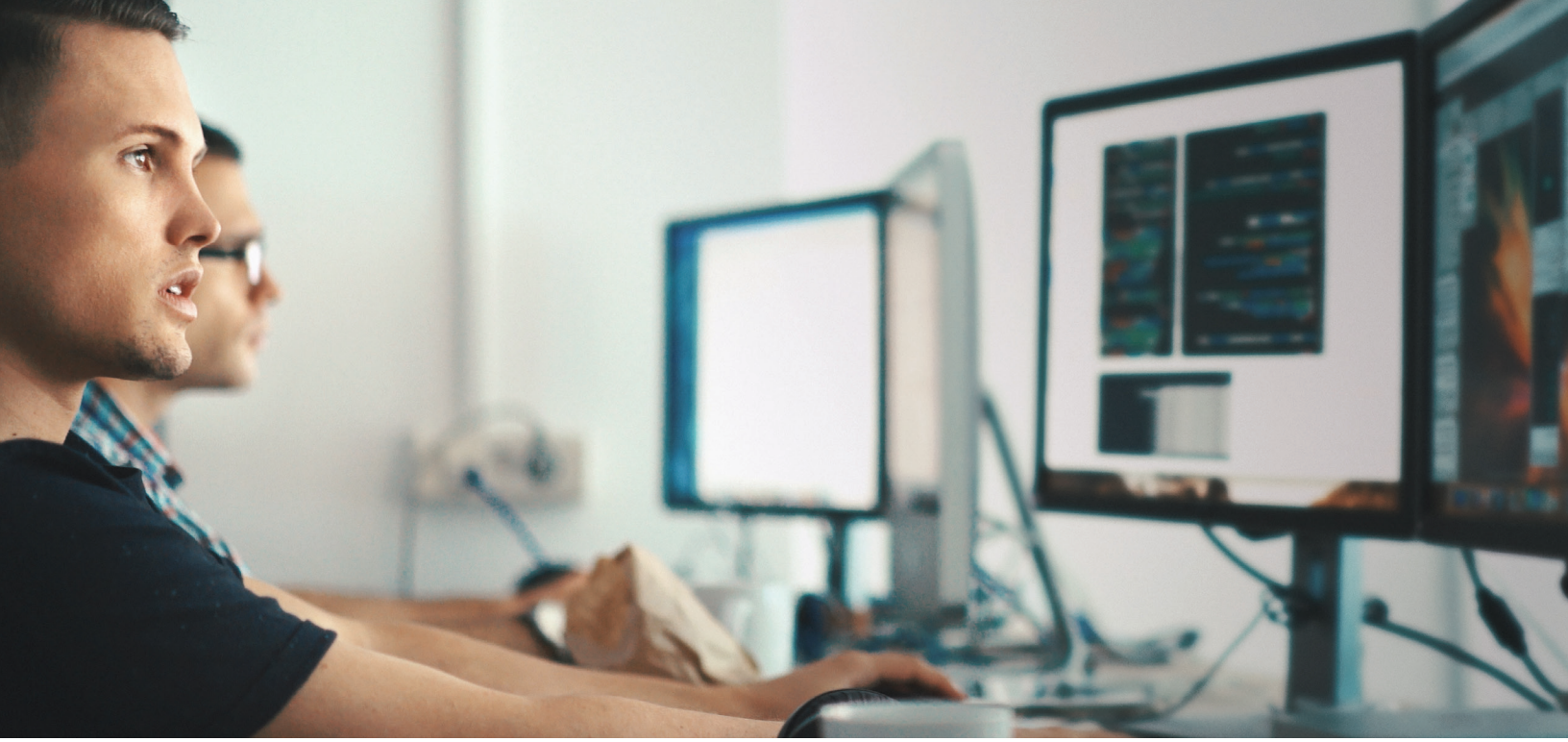


DIGITAL INDUSTRIES SOFTWARE

Questa Base

Benefits

- Reference simulator on LRM compatibility
- Native compiled, single kernel simulator technology
- VHDL, Verilog, SystemVerilog, and mixed language support
- Superior debug with Visualizer
- Simulation in advanced optimization mode
- Code coverage
- SVA and PSL assertions
- Coverage collection for SVA and PSA
- Profiling for hotspot analysis
- C code debug

Sophisticated FPGA verification

Questa™ Base packs unprecedented verification capabilities in a cost-effective HDL simulation solution. Its award-winning single kernel simulator (SKS) technology enables the transparent mixing of VHDL and Verilog in one design. Questa Base simulates behavioral, RTL, and gate-level code, including VHDL VITAL and Verilog gate libraries, with timing provided by the standard delay format (SDF). The Questa Base architecture allows platform-independent compilation with the outstanding performance of native compiled code. Design quality and debug productivity are improved with the state-of-the-art Visualizer debug solution.

The graphical user interface is powerful, consistent, and intuitive. You can edit, recompile, and re-simulate without leaving the Questa Base environment. All windows update automatically following activity in any other window. For example, selecting a design region in the structure window automatically updates the source, signals, process, and variables windows. All user interface operations can be scripted, and simulations can run in batch or interactive modes.

Benefits *continued*

- Intelligent, easy-to-use GUI with Tcl interface
- Integrated project management, source code templates, and wizards
- Wave viewing and comparison; objects, watch, and memory windows increase debug productivity
- 64-bit support for Linux and Windows

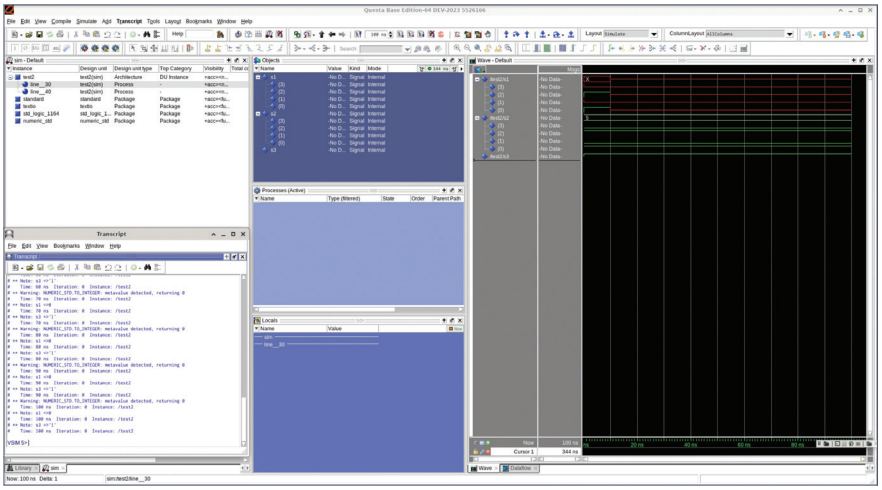
Platform support

- Windows and Linux (64-bit)
- Windows 10, Linux RHEL 7 and 8, and Linux SLES 12 and 15 *

*Please refer to the licensing and installation guide in the latest documentation of your Questa Base release.

Assertion-based verification with SVA and PSL

Assertion-based verification (ABV) improves design quality by inserting white-box monitors that provide a window allowing active monitoring of functional correctness. Assertions catch errors that tests activate but fail to propagate to typical black-box observation points, such as the primary outputs. The assertions also turbocharge time-to-debug productivity by identifying functional bugs much closer to the root cause. The time savings from a significantly shorter causality traceback can amount to hours or even days. Questa Base enables ABV by supporting SystemVerilog Assertion (SVA) constructs and the Property Specification Language (PSL). SVA and PSL assertions can be either embedded within the design HDL source code or specified in separate units, then bound to the appropriate module instance in the design hierarchy.



Questa Base offers the most verification capabilities and the highest debug productivity in its class.

Code coverage

Design verification completeness can be measured through code coverage. Questa Base supports statement, expression, condition, toggle, and FSM coverage. Code coverage metrics are automatically derived from the HDL source. As many design blocks are created to be configurable and reusable and not all metrics are valuable, code coverage metrics can be flexibly managed with source code pragmas and exclusions specified in the code coverage browser.

Advanced optimization and productivity flow

Questa Base supports advanced optimization algorithms that can significantly improve simulation performance. Questa Base achieves industry-leading performance and capacity through aggressive global compile and simulation optimization algorithms for SystemVerilog and VHDL. It also supports fast turnaround time flows and effective library management, while maintaining high performance, through unique preoptimization and reuse capabilities. Users can turn on performance optimization and run the optimized simulation image to achieve faster simulation turnaround times.

Questa Base also supports the Qrun flow to improve compilation turnaround and simplify simulation runs. Qrun is a single flow "wrapper" that automatically invokes the appropriate VHDL or Verilog compiler and optimizer based on the command line arguments. The Qrun arguments are dispatched to the correct tools without the user having to know which switch goes to which tool.

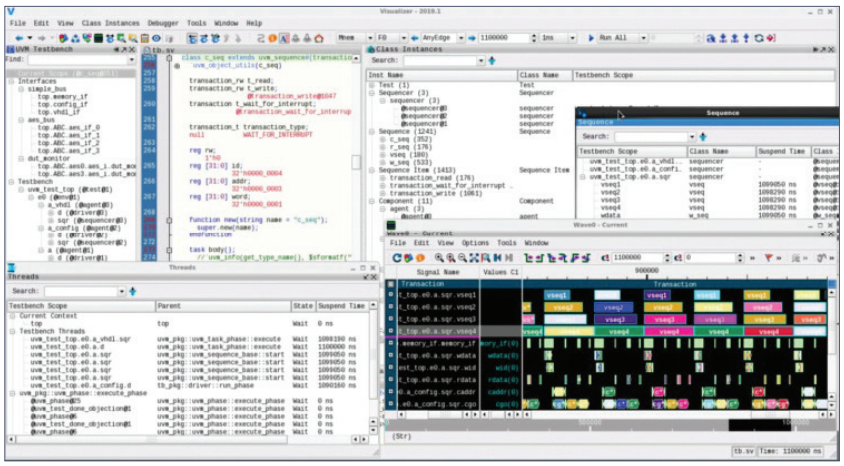
Maximizing the efficiency of RTL verification often requires analyzing simulation runtime performance to look for bottlenecks and potential improvements. With RTL profiler enabled, engineers can identify the design's hot spots – the instances, modules, or lines of code that impact simulation performance.

Premium debug – Questa Visualizer

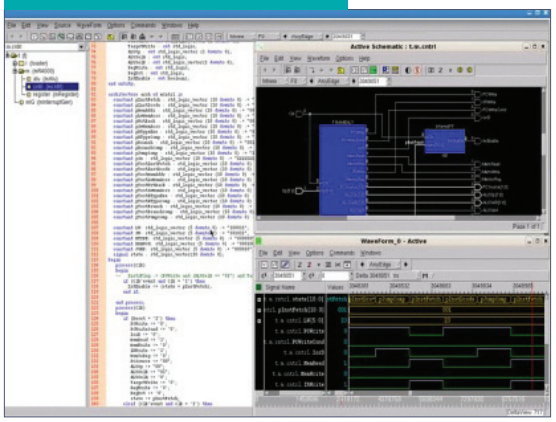
For years the process of ASIC and FPGA design and verification debug consisted primarily of comprehending the struc¬ture and source code of the design with waveforms showing activity over time, based on testbench stimulus. Today, functional verification is exponentially complex with the emergence of new layers of design requirements (beyond basic functionality) that did not exist years ago; for example, clocking requirements, security requirements, safety requirements, and requirements associated with hardware-software interactions. Given these complex interactions, effective debug often demands experts that are familiar with all the components and a debug environment that is aware of these heterogeneous requirements. According to the 2022 Wilson Research Group Verification study, design and verification

Comparison of Questa Base against ModelSim DE

	Questa Base	ModelSim DE
SVA	Y	Y
PSL assertions	Y	Y
Checkpoint and restore	Y	N
Advanced FSM debug	Y	N
Coverage collection SVA PSA	Y	N
Performance profiling	Y	option
Visualizer (premium debug)	Y	N
C Code debug	Y	option
Performance optimization	Y	N
Post simulation debug	Y	option
Qrun	Y	N
Verilog simulation	Y	Y
VHDL simulation	Y	Y
Mixed language simulation	Y	option
Code coverage	Y	Y
Interactive waveform	Y	Y
Schematic viewing TK GUI	Y	Y
Dataflow in TK GUI	Y	Y
Windows	64 bit	32 bit
Linux	64 bit	32 bit



Interactive and off-line



The Questa Visualizer single environment for testbench and RTL DUT debug.

engineers now spend 47% of their overall project time debugging – and that percentage is growing. A strong debug solution is necessary to improve debug productivity.

Questa Visualizer is a context-aware debug platform that supports a complete logic verification flow, including simulation, emulation, and prototyping, as well as design, testbench, low-power, and assertion analysis. It has intuitive features with powerful design and verification debug capabilities for debugging in live- or post-simulation modes. Visualizer provides a high-performance, high-capacity debugger that scales from simulation to emulation. Multiple automated features quickly find RTL, gate-level, and protocol bugs. Low-power debug using the Unified Power Format (UPF) is fully integrated and overlaid with RTL views. Visualizer is SystemVerilog class-based and UVM-aware to speed up overall debug time, even on today's most complex SoCs and FPGAs.

Further resources

Siemens EDA Verification Expertise provides sample resources to help you get started adopting advanced verification techniques.

The Verification Academy is organized into a collection of free online courses and resources, focusing on key aspects of advanced functional verification designed to mature an organization's verification process. Course topics include assertion-based verification, clock-domain crossing verification, formal assertion-based verification, formal coverage, metrics in SoC verification, portable stimulus, power-aware simulation, UVM debug, and much more. Each course consists of multiple sessions allowing the viewer to pick and choose topics of interest and revisit topics for future reference.

The Verification Academy is the complete UVM online resource collection. You will find everything you need to get up to speed on UVM, whether downloading the kit(s) or participating in online or in-person training. The UVM courses provide an excellent overview of methodology concepts – from introductory to advanced levels – with videos that walk you through helpful code examples. The UVM Online Methodology Cookbook is an online textbook to show you in more detail how to use the various features of the methodologies to create reusable verification components and environments.

Consulting and Training. Siemens EDA Consulting Verification Services offers solution-driven consultants that dramatically reduce your verification process times while improving quality. Unlike other EDA consulting services or third-party consultants, Siemens EDA Consulting's highly experienced Verification Services team offers customized solutions and proven, structured processes to ensure projects are delivered on time and to specification, with a greater probability of first-pass success. Siemens EDA Education Services offers a full range of learning solutions developed specifically for electronics designers and engineers engaged in advanced verification. Users can choose the type of training that best suits their needs and schedule. These choices include unique live online training as well as training and seminars at Siemens EDA training centers worldwide and on-site training and mentoring tailored to your company.

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